ATLAS
Level–1 Muon Barrel
RODbus
Preliminary Design Review

Mar.12, 2002

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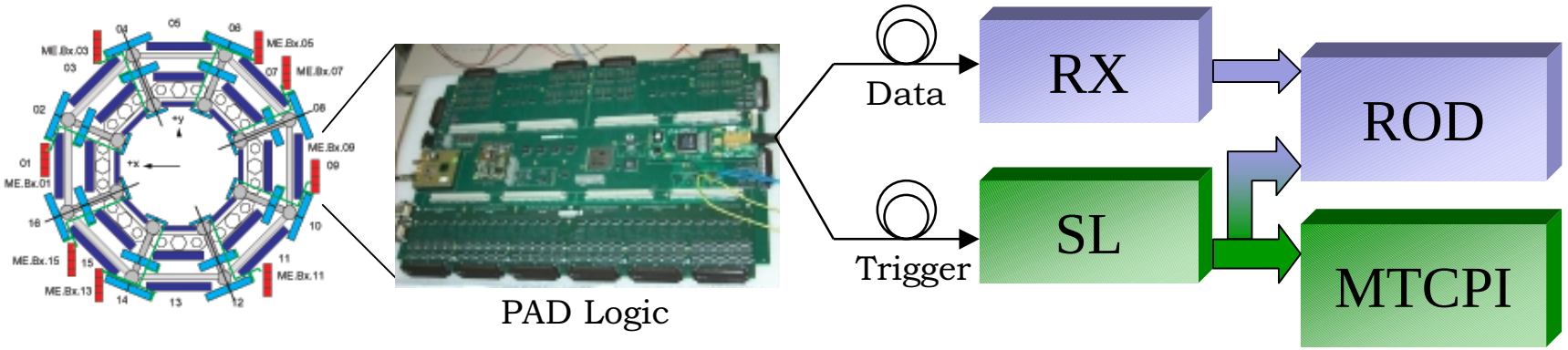
Overview

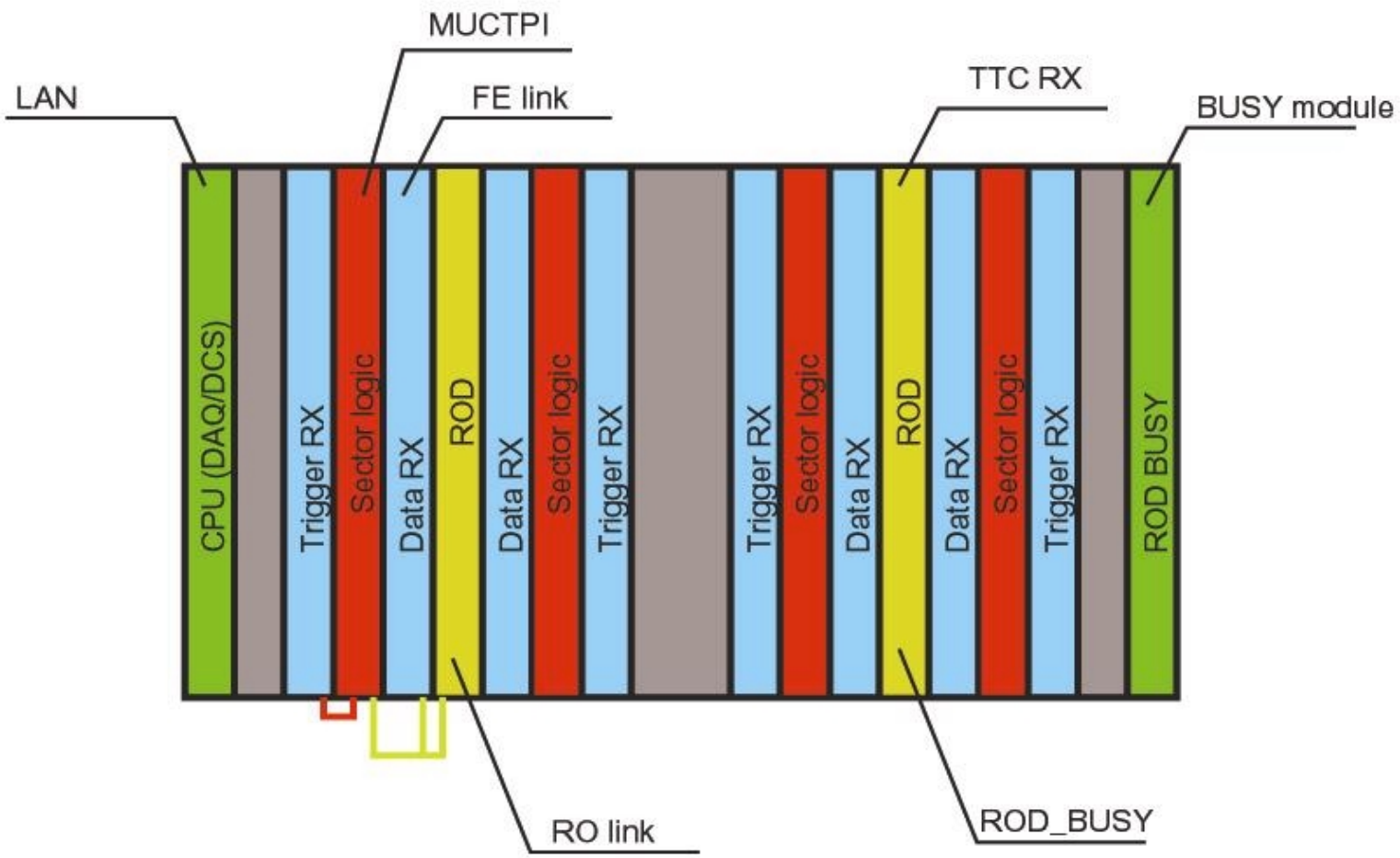
- Muon Level-1 Trigger and Data path
- ROD crate architecture
- RODbus features
- Measure, models & simulations
- Test results
- Conclusions

From PAD to ROD/SL

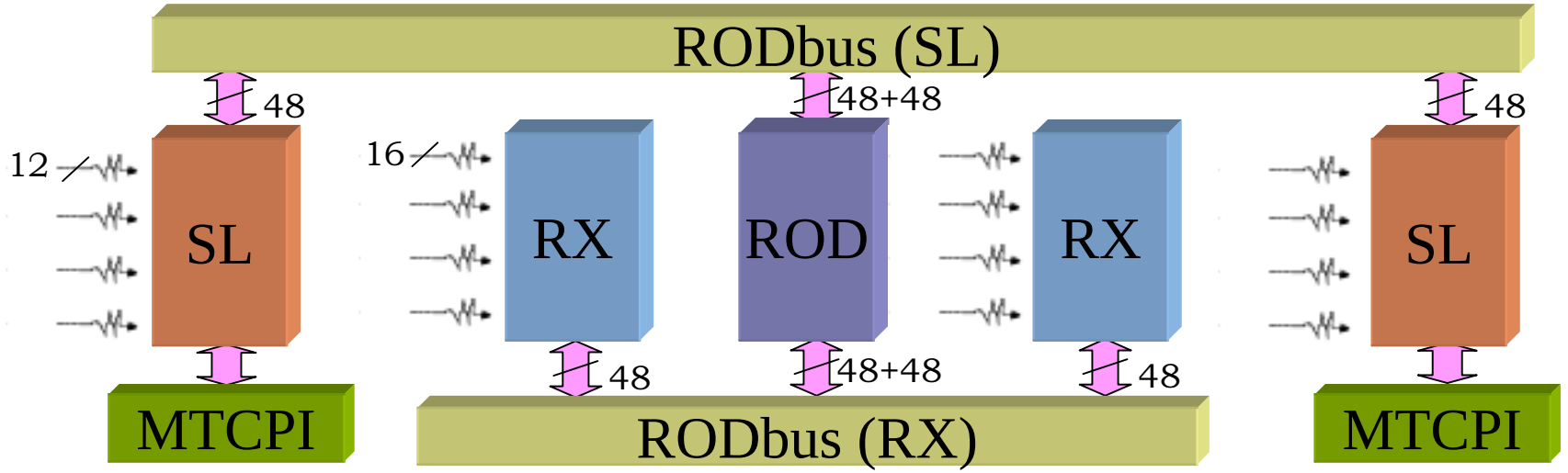


- Optical out from PAD to:
  - SL
  - ROD
- 12 bit @ 40MHz on the trigger path; synch, fixed and low latency link required to guarantee timing.
- 16 bit + strobe on the data path.

ROD Crate layout



RODbus requirements

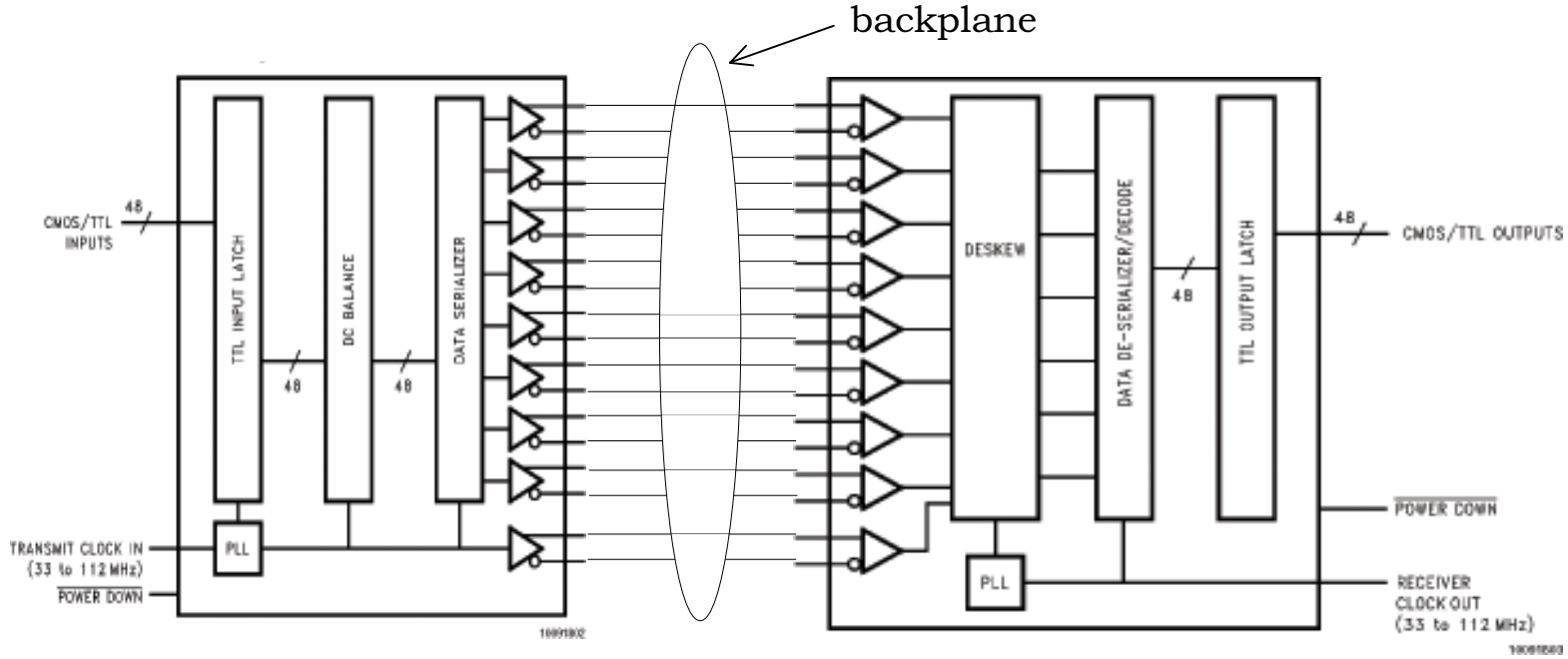


- SL to ROD
  - 48 bit@40MHz
  - synchronous with low latency
- RX to ROD
  - (16+8 bits x 2 = 48 bits)
- ROD to RX/SL (not shown)
  - Low skew, low jitter clock distribution
  - control signals (RST*, LVL1A, ...)

Strategy

- Common platform for both SLs and RXs to ROD backbones:
  - SL asks for a synchronous design.
  - Low skew, low jitter signals need a differential signaling scheme.
  - Doubling data lines saturates the pin availability (and board space) if a SerDes approach is not used.
  - Low voltage, low power (and high performances) suggest LVDS.
  - System level “non-timing” signals (as RST*) can run TTL.

Choosing the chip-set

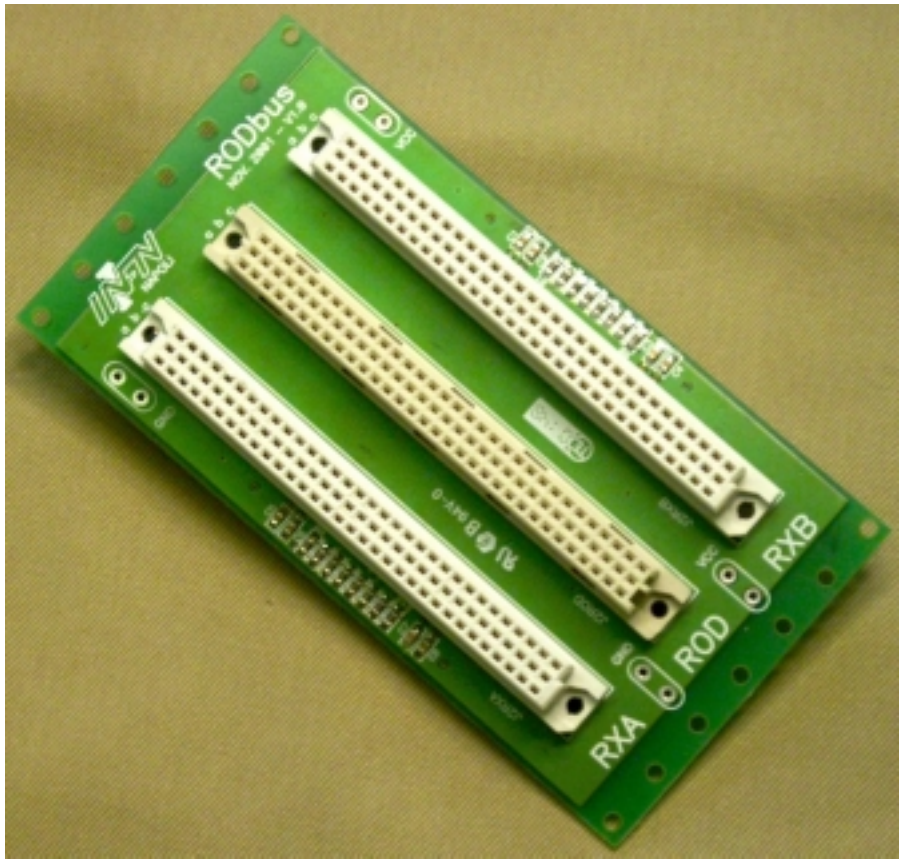


- DS90CR483/4 chip-set, a 48:8 bit + clock LVDS pseudo SerDes
- Deskew and Preemphasis for improved performances
- Data transfer rate @ 7x master clock frequency

Partitioning the problem

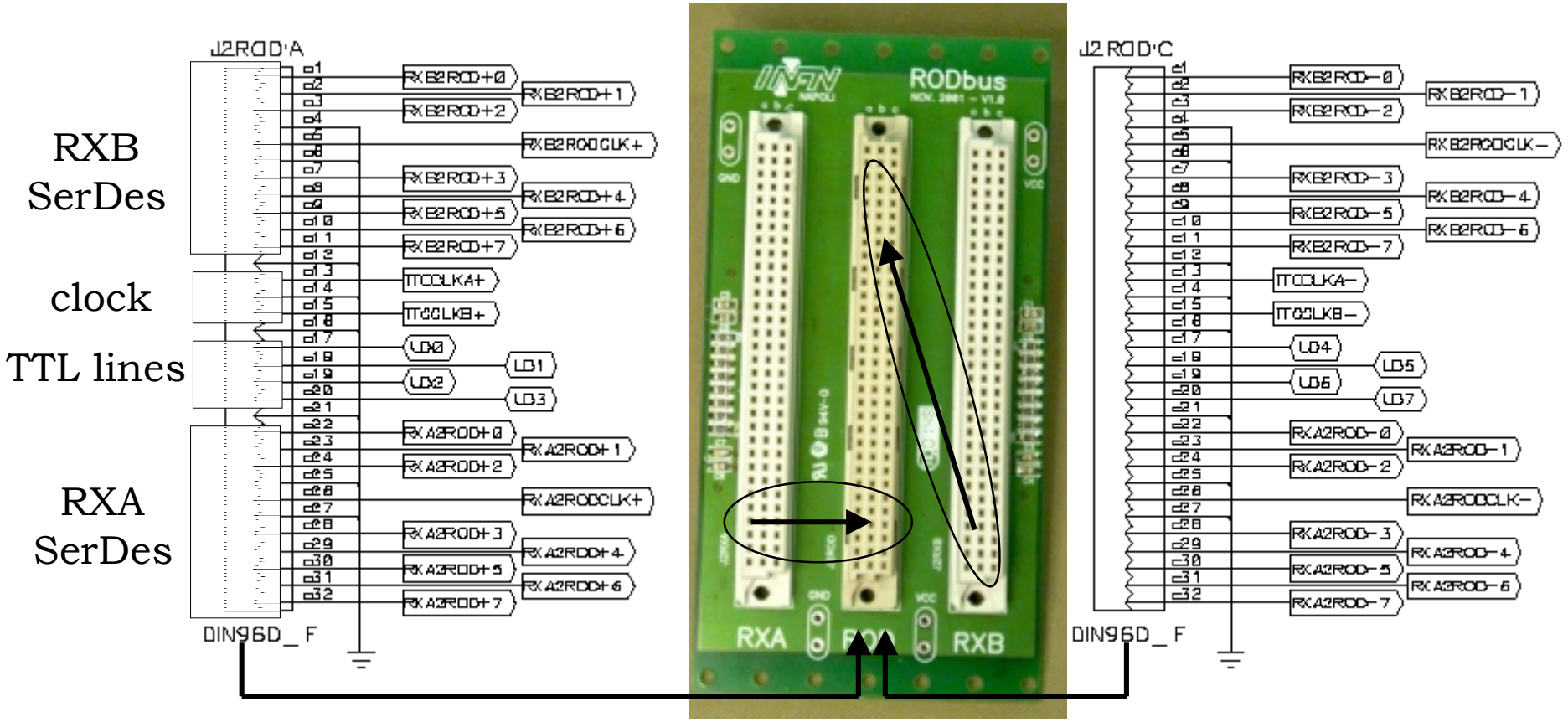
- To optimize board layout and backplane performances, we decided to assign the SLs to ROD and the RXs to ROD channels to two “add on” backplanes.
- In this review, we present the prototype of the RXs to ROD backplane, assigned to J2
- The SLs to ROD backplane will be done using the same technology, mapped to J0

RODbus: RXs to ROD



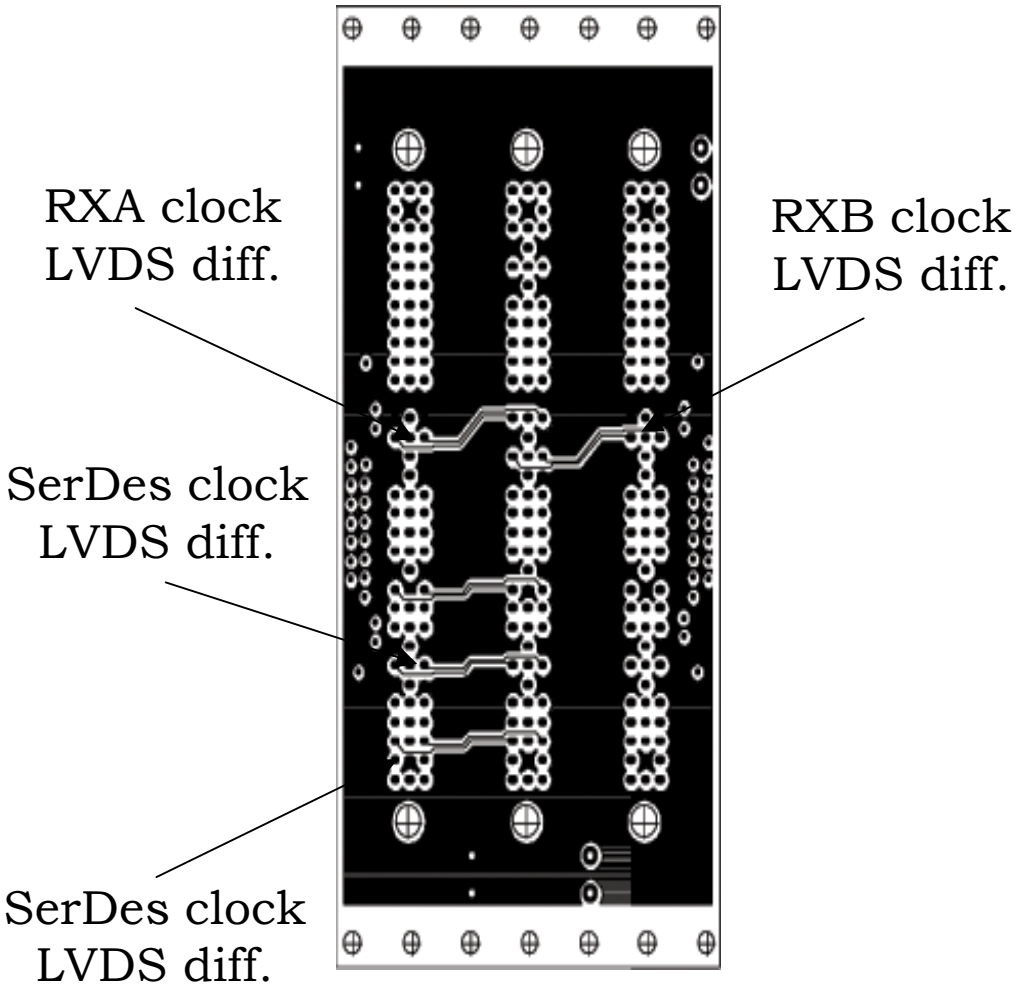
- 3 slot backplane to link 2 RXs to one ROD
- 10 layer stack-up
- Diff. microstrip for LVDS pairs and single ended for TTL lines on separate planes
- Plug-in to the VME64 rear side. TTL lines terminated as VME

ROD slot pinout



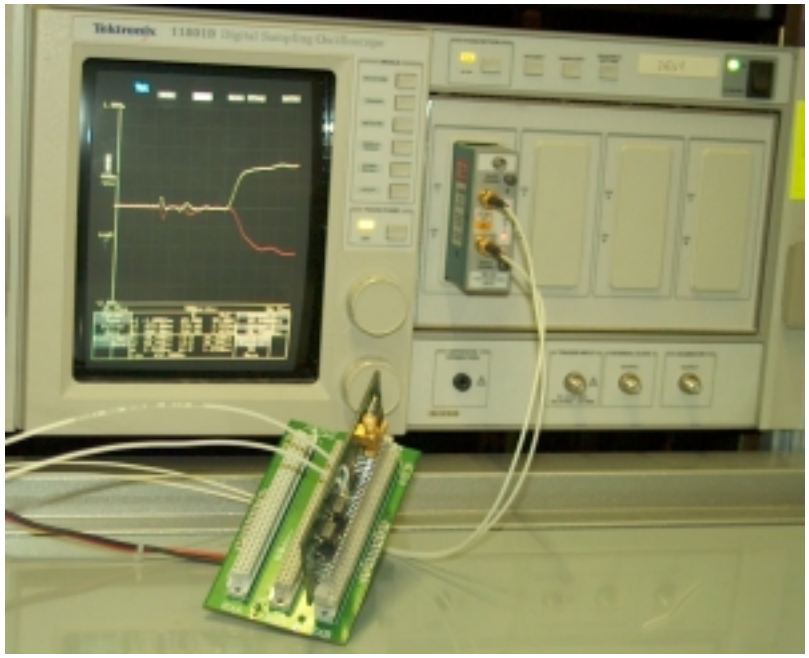
- ROD distributes clock and 8 system control signals
- Receives 48bits@40MHz from each adjacent RX

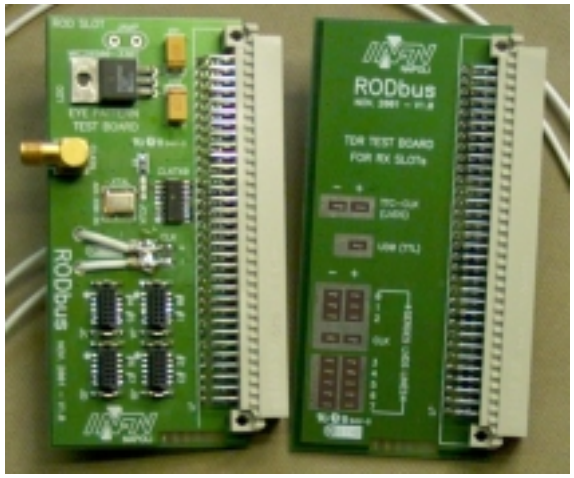
Physical layout



- Diff. LVDS pairs routed as edge coupled microstrips
- All pairs have the same length (10 mil tolerance).
- Noisy TTL lines are routed on a separate plane.

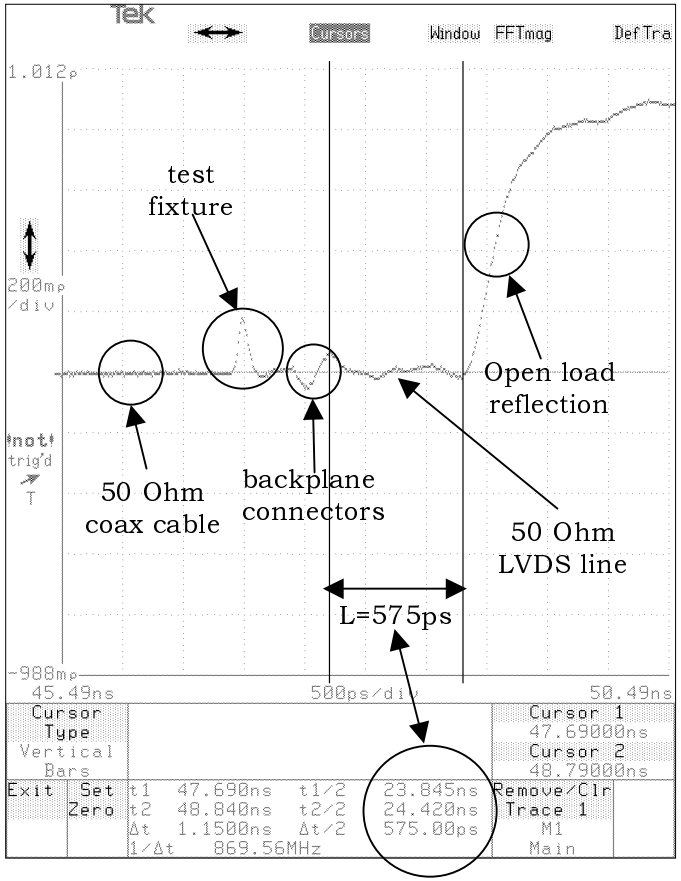
TDR interface





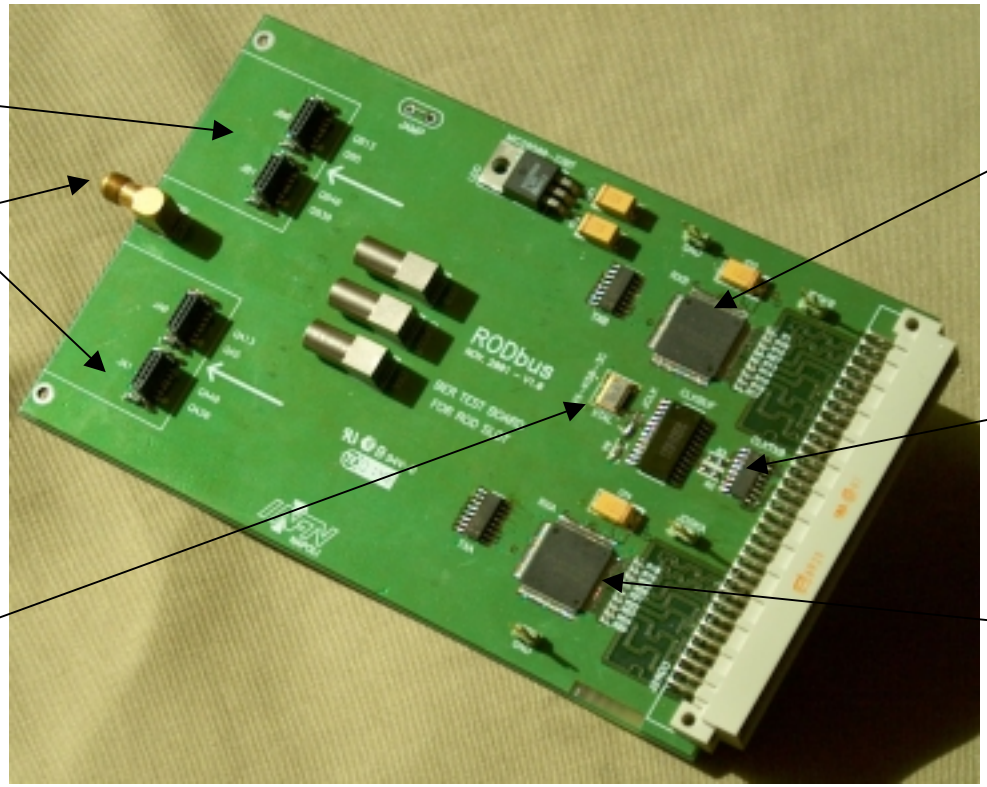
- Two test fixtures have been designed to interface the RODbus to TDR
- Diff. Impedance profile can be measured
- Impact of connectors, vias, stubs and holes (present in the real environment) can be evaluated

TDR profile



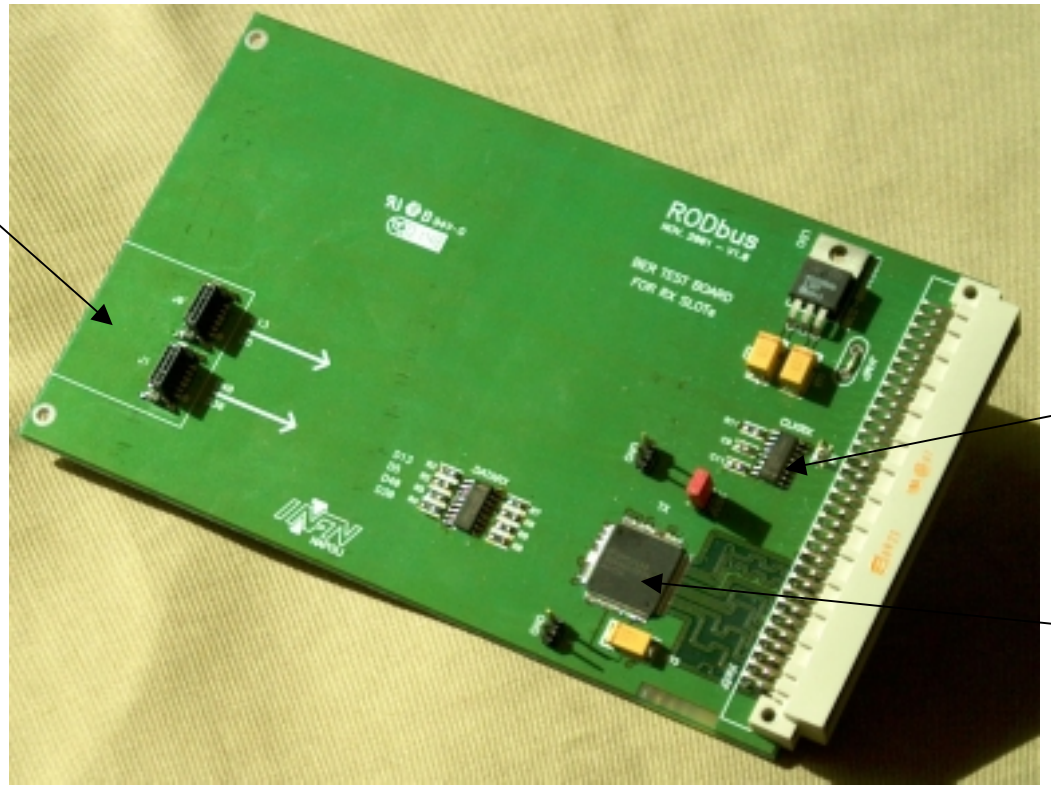
- TDR step probes backplane line and connectors
- PCB stack-up is tested
- line length and impedance are measured
- lumped L/C (connectors, vias, solder pads) are visible

Testing the SerDes: ROD slot



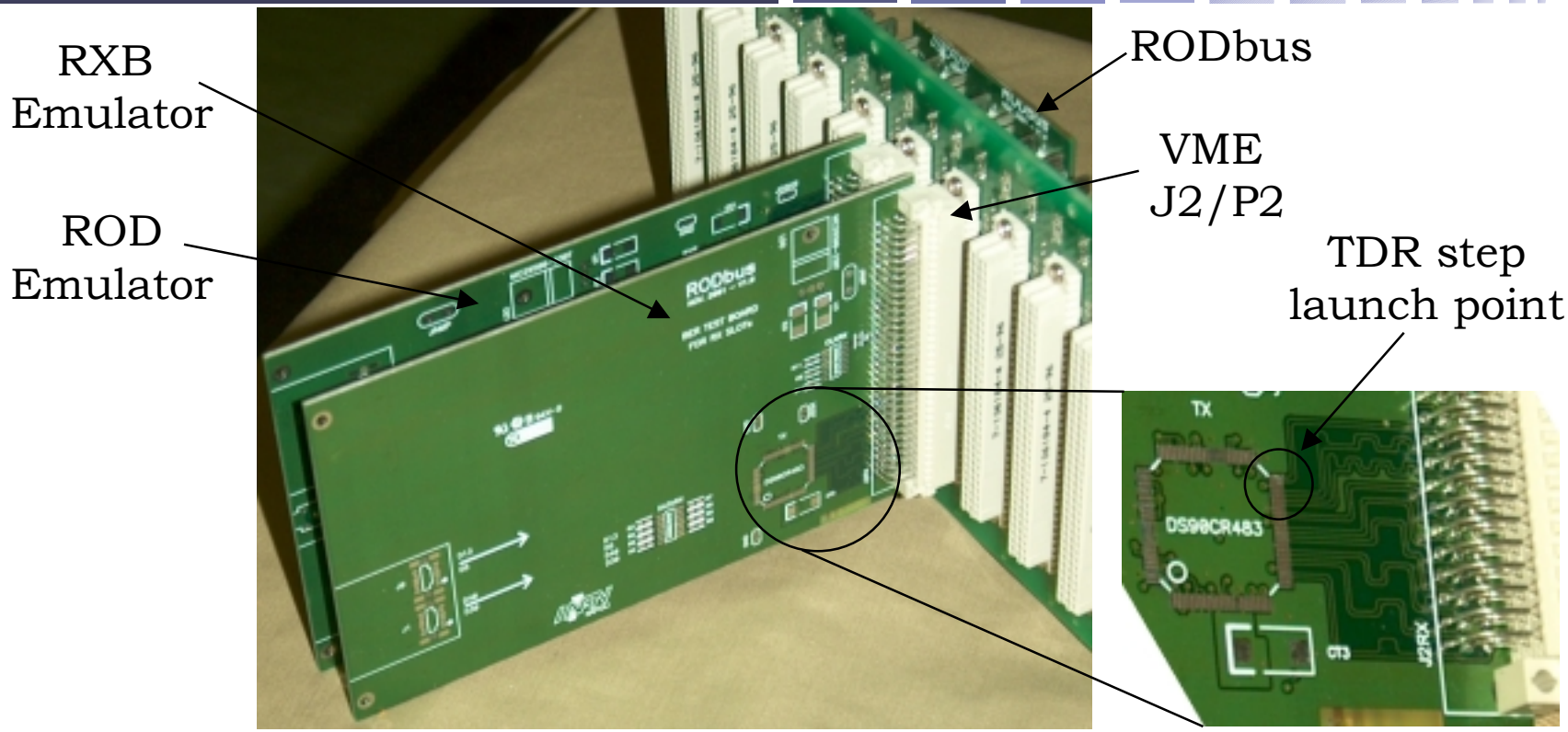
- ROD emulation:
  - Distributes Clock to RXs (from ext. or local source)
  - Receives serial streams from RXA and RXB

Testing the SerDes: RX slot



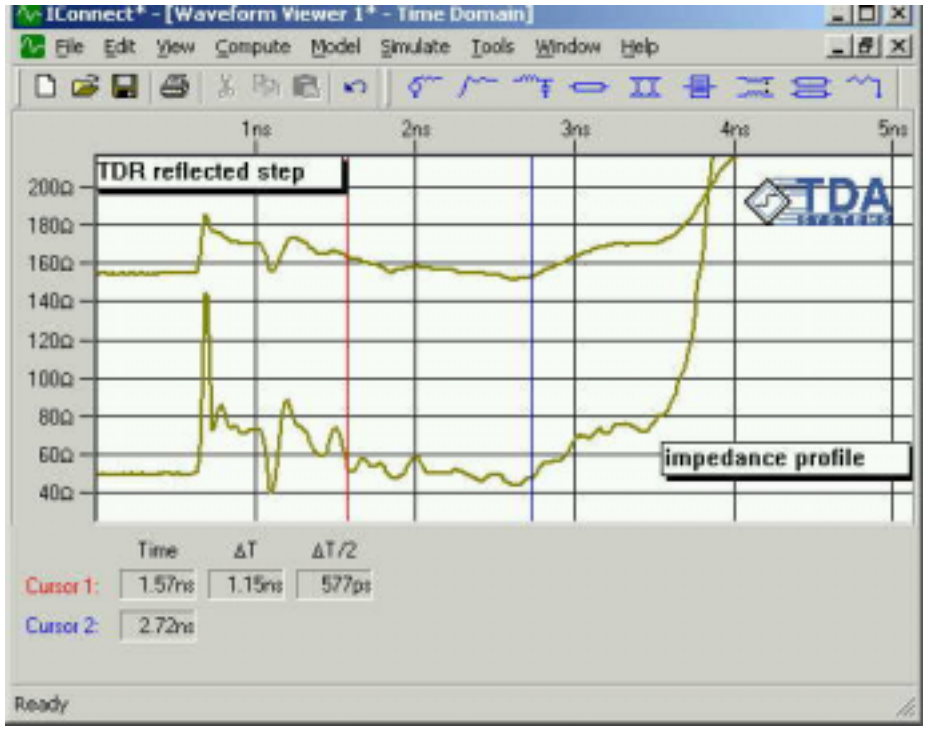
- RX emulation:
  - Receives Clock from ROD
  - Transmits serial streams to ROD

TDR system test



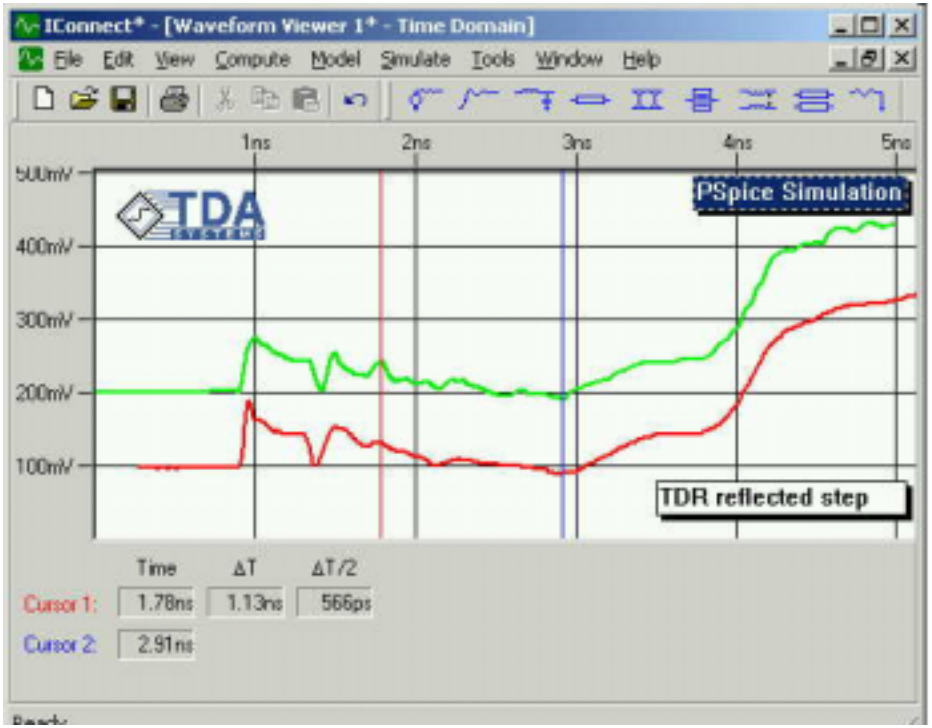
- The entire RX-to-ROD connection is analyzed
- Unpopulated RX and ROD emulators are used to evaluate the signal integrity using TDR

Impedance profile



- The TDR reflected step shows the discontinuities (vias, holes, connectors, ...)
- The impedance profile is derived deconvolving the multiple reflections

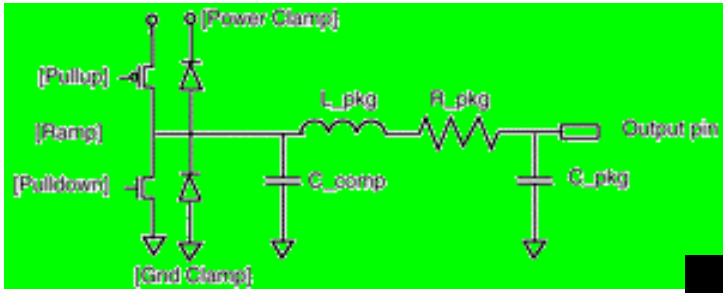
Modelling the system



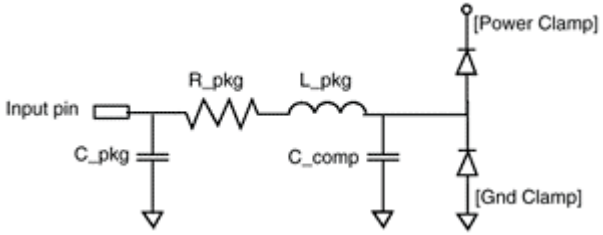
- A PSpice model has been developed, based on the impedance profile
- The model is based on ideal (lossless) line segments

- Model validation is performed by simulating the TDR reflected step. Results are in excellent agreement with experimental data

IBIS models



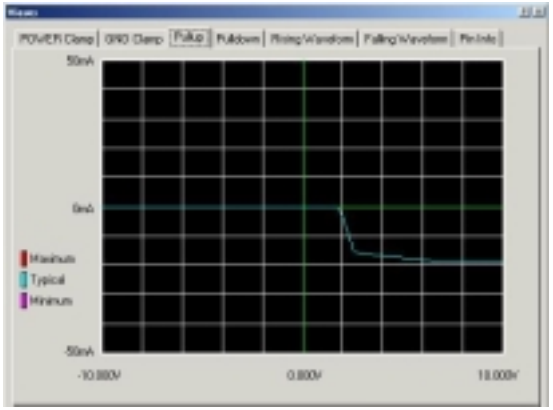
Typical output stage

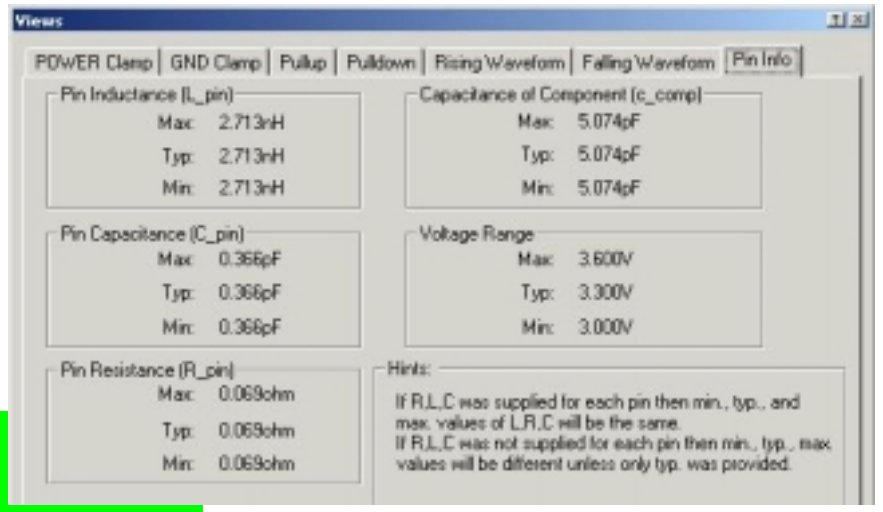


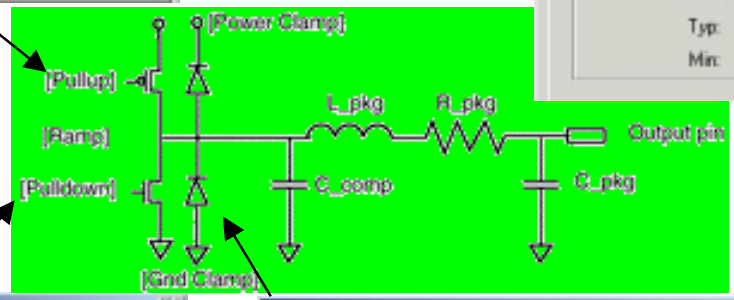
Typical input stage

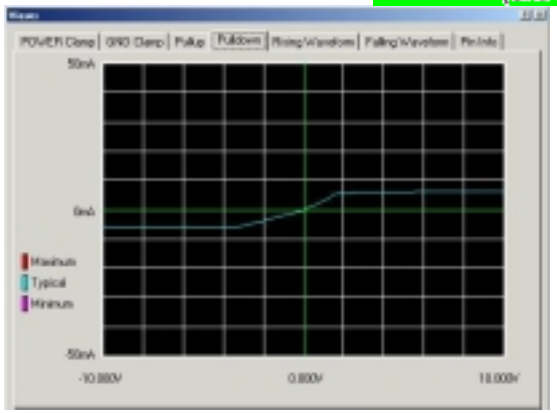
- IBIS is an ANSI standard to model I/O buffers mainly for signal integrity issues
- Different from SPICE, IBIS gives only a behavioral description - disclosing no proprietary circuit information
- The I/O buffer is characterized by means of a standard template of VI curves and stray L,C and R

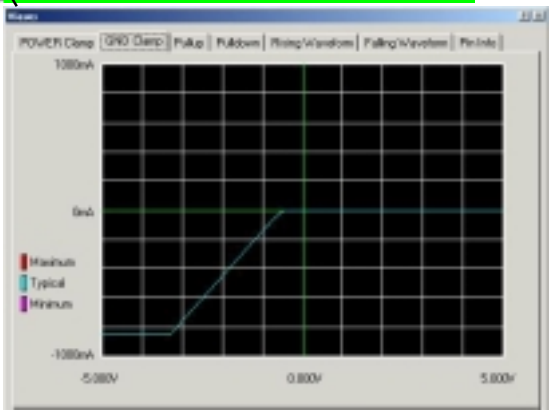
DS90CR483 LVDS Output



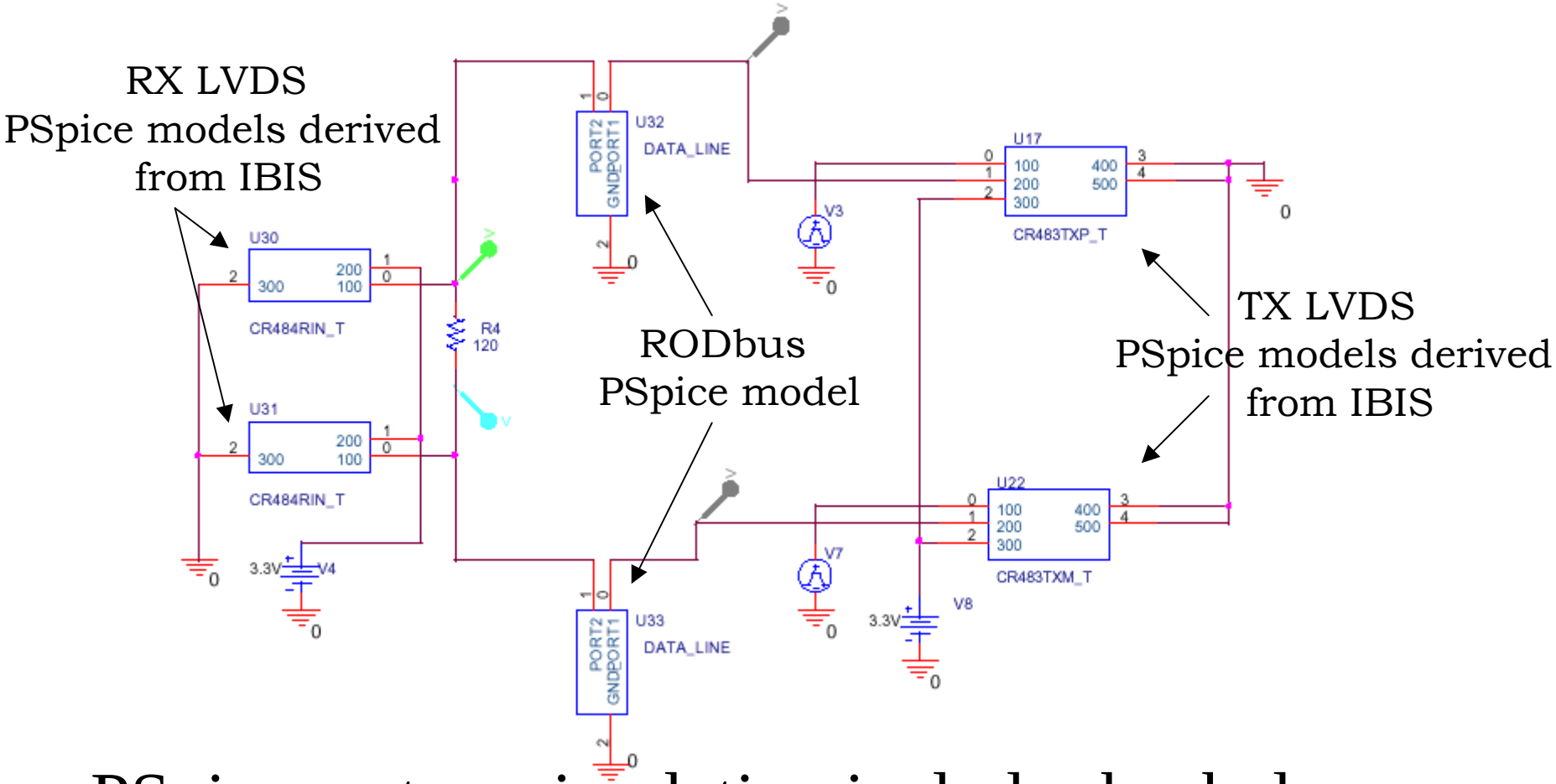








System simulation

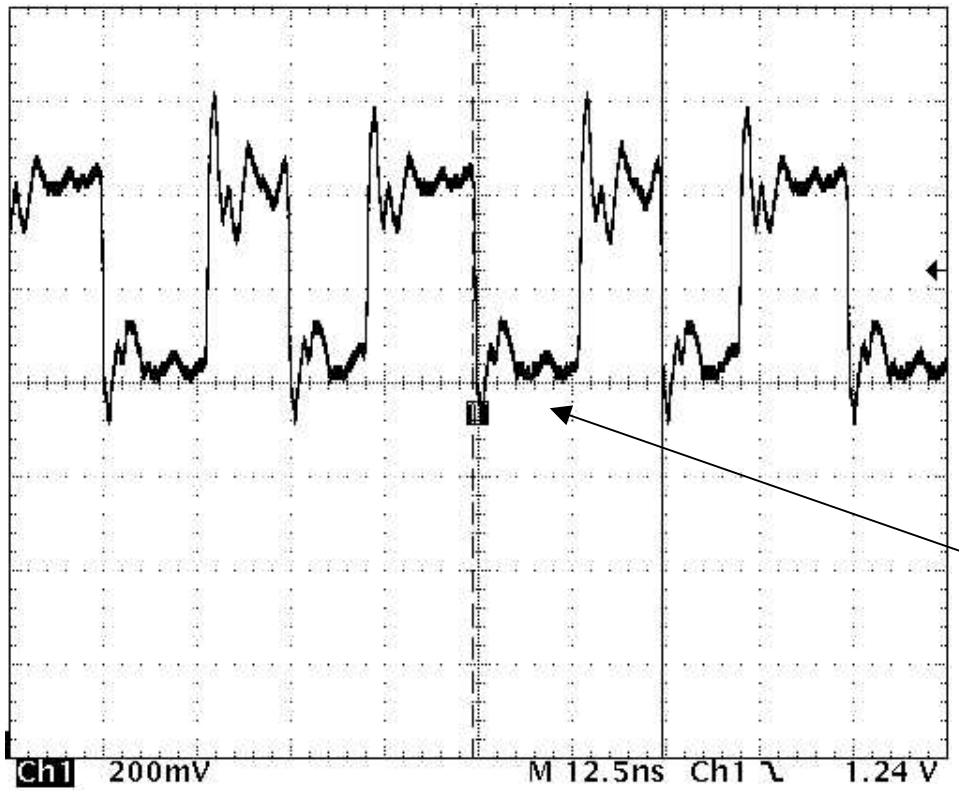


- PSpice system simulation includes backplanes, connectors, stubs, SerDes TX and RX

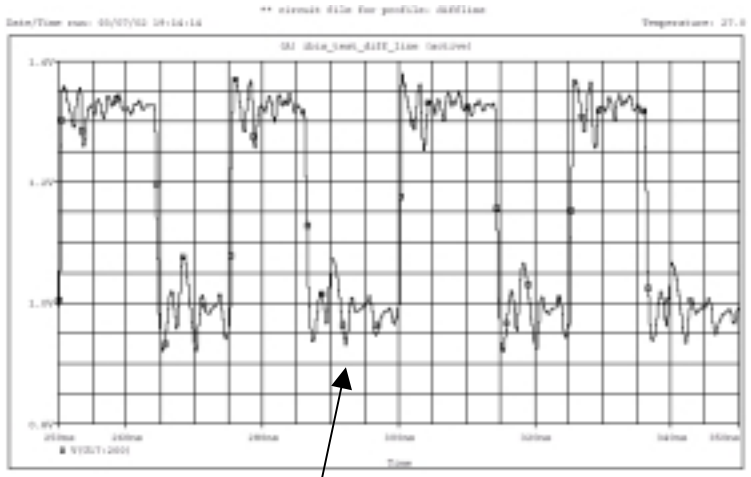
Simulation caveat

- Interconnection Model is based on ideal transmission lines
- Crosstalk, ground bounce, probe loading are not modeled
- TDR-derived models are less accurate the longer the step travels
- SerDes IBIS model only specs typ. values, pre-emphasis and deskew not modeled
- Standing wave needs long simulation runs (>15h to simulate 2us on a Pentium II – 350)

SerDes LVDS clock - TX side

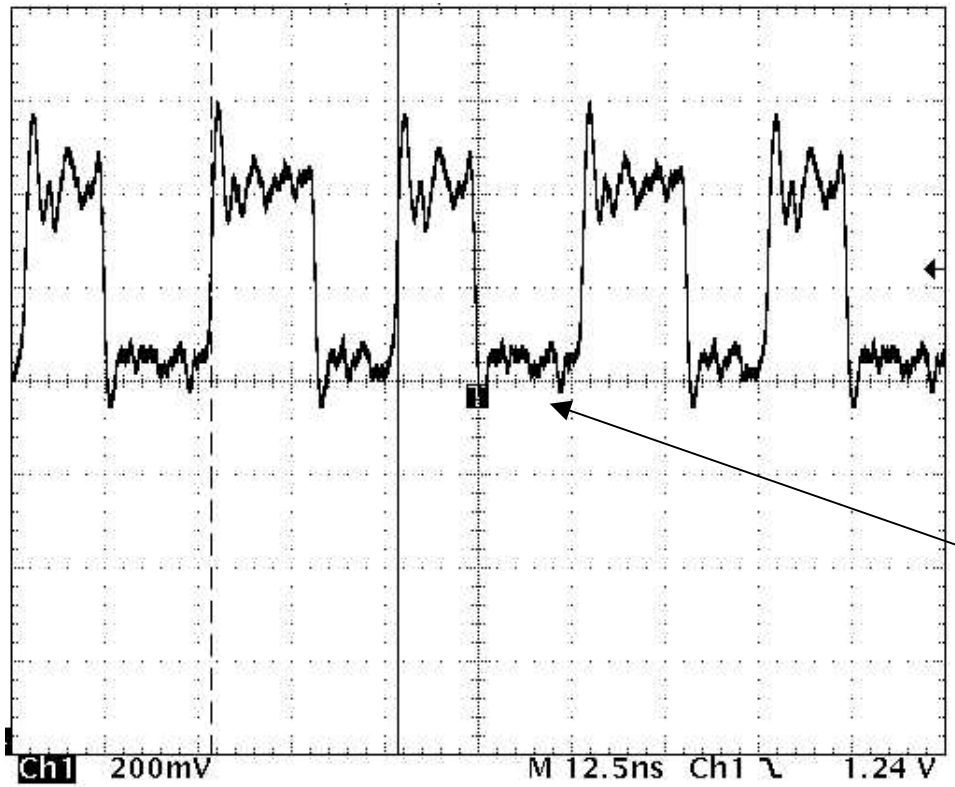


simulation

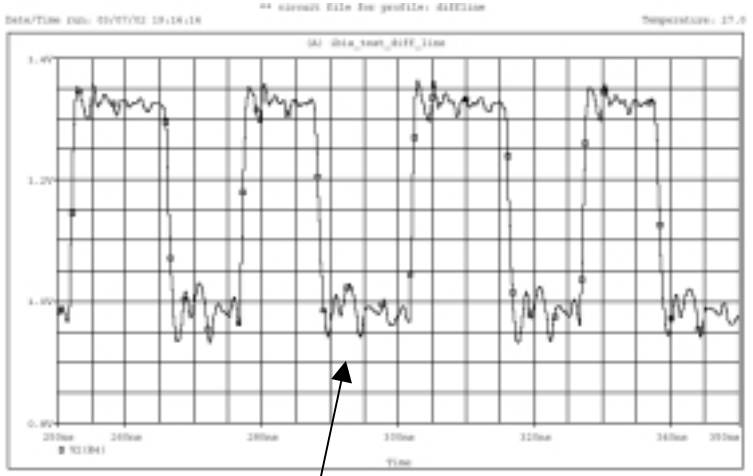


LVDS SerDes
Clock @ TX

SerDes LVDS clock – RX side



simulation



LVDS SerDes
Clock @ RX

Test results (preliminary)

- Tests with 2^15 PRBS show no errors in the SerDes operations up to 60 MHz (420 Mbit/s). Fine tuning should allow reaching 80 MHz (560 Mbit/s).
- Latency is 5 clock cycles (125ns @ 40 MHz), dominated by the SerDes specs. RODbus T_{pd} (570 ps) is negligible.

More tests to be done

- RODbus performances in a real VME (noisy) environment
- EMI
- BER vs. clock frequency and different patterns
- 48-bit 2^16 Pseudo Random Word Sequence (PRWS) test requires a custom platform (generator, analyzer, adapters, …) to be developed

Conclusions (1/2)

- RODbus is the proposed backbone for all the ROD crate interconnection needs
- It specifies the physical layer (backplane, line impedance, levels) and the logical layers (SerDes specs)
- Data transfer rate is 7x the master clock frequency (280 Mbit/s @ 40MHz) requiring careful PCB layout for backplane and users' boards. Emulators have been designed proof of concept, tests and PCB layout reference

Conclusions (2/2)

- RODbus has been in-deep characterized by using TDR techniques. SPICE models have been derived and validated. SerDes SPICE models have been crafted starting from IBIS files.
- The entire system has been simulated with PSpice and results show good agreement with experimental data.
- Analog simulations has been successfully used to evaluate the system performances and signal integrity issues.