ATLAS Level–1 Muon Barrel Optical Link Final Design Review

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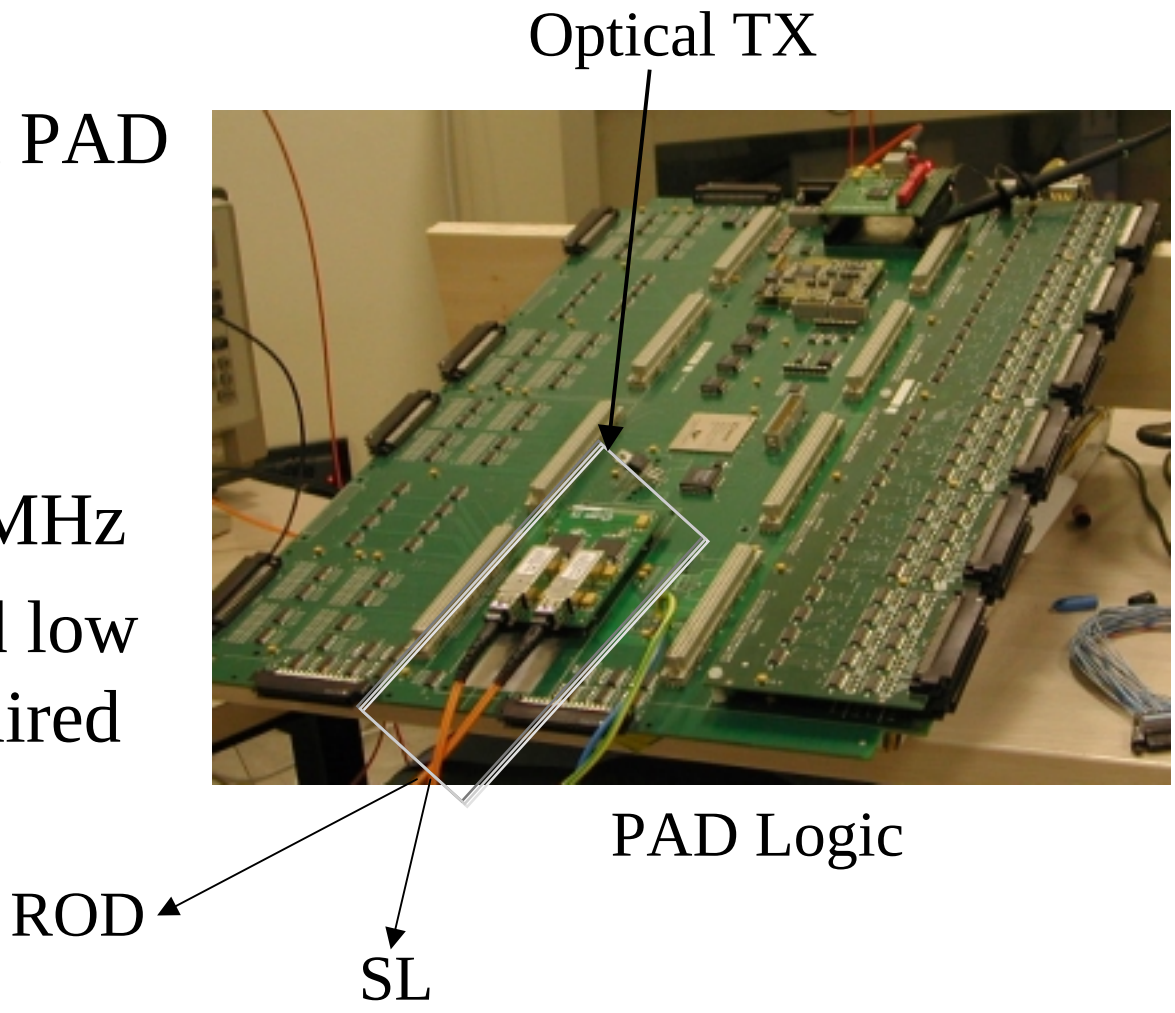
Overview

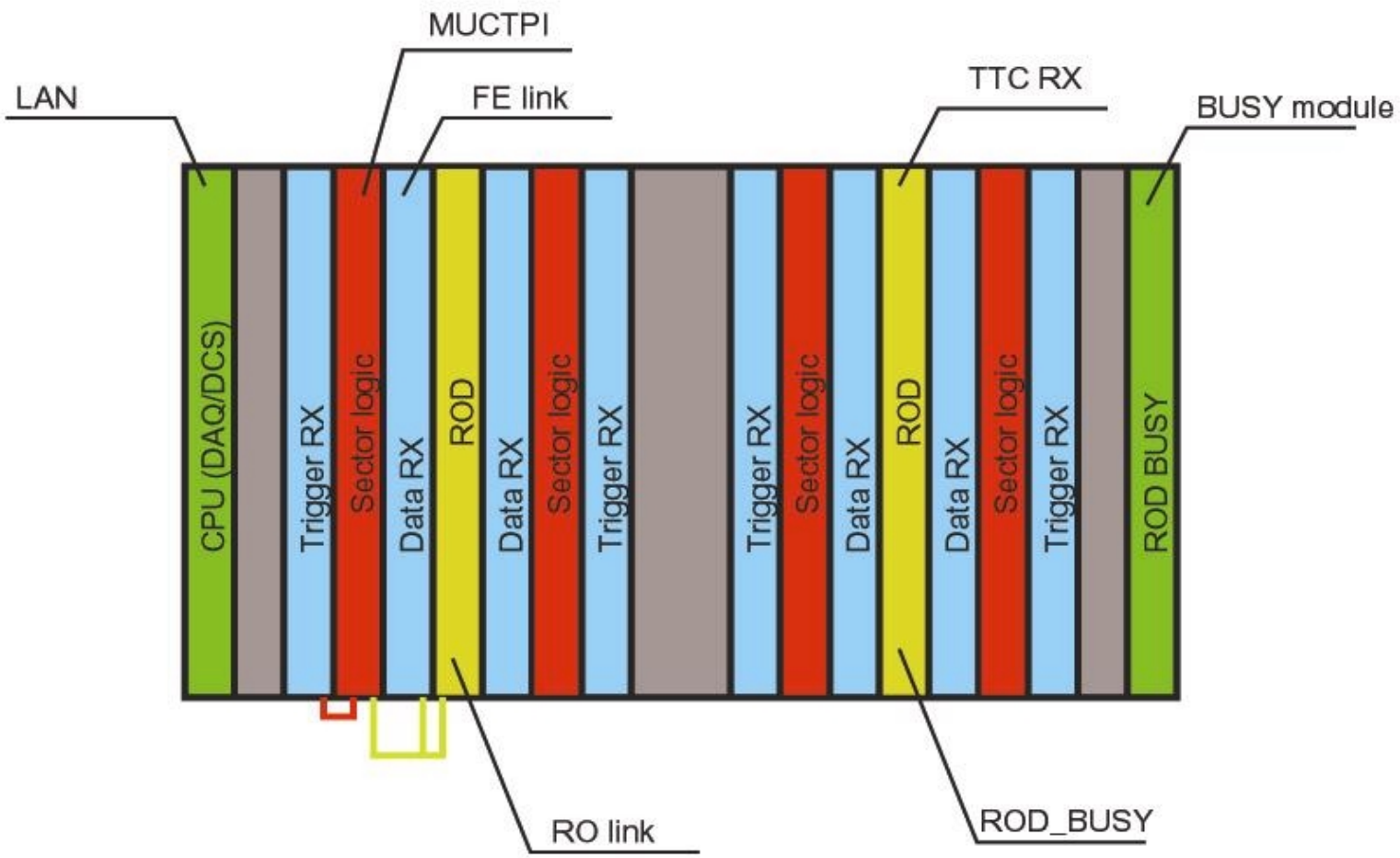
- Optical links in the Muon Level-1 Trigger and Readout
- Status at PDR (Nov. 2001)
- PAROLI trend
- G2LINK test results
- Conclusions

From PAD to ROD/SL

- Optical out from PAD to:
  - SL
  - ROD
- 16+16 bit @ 40MHz
- Synch, fixed and low latency link required



ROD Crate layout



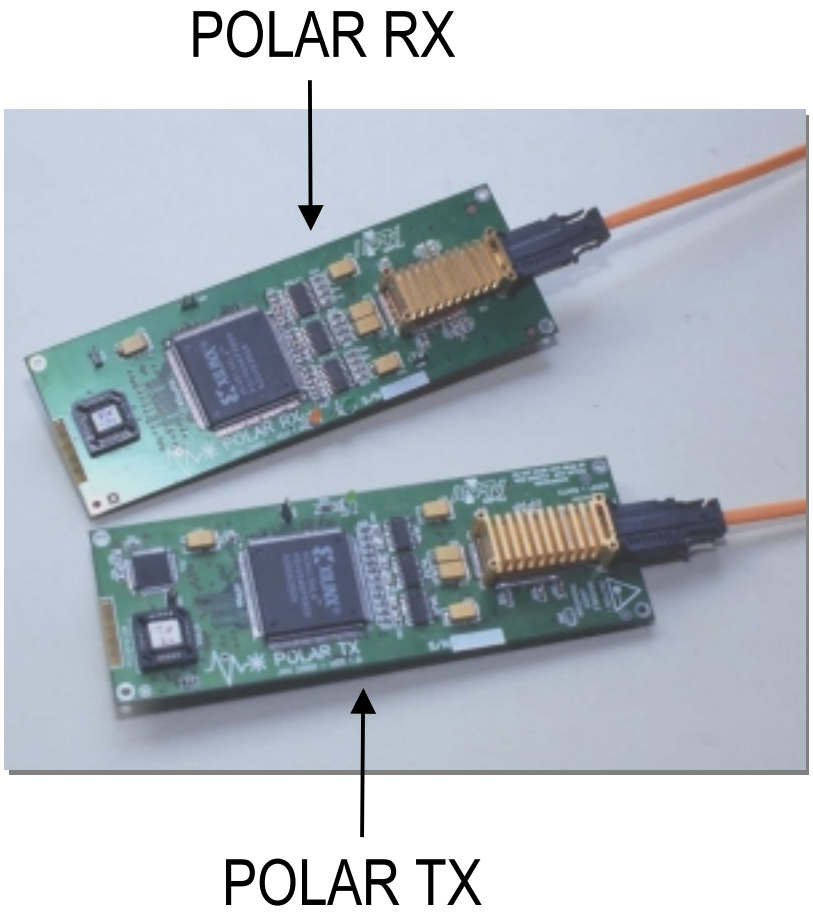
Conclusions @ PDR (1/2) (Nov. 2001)

- Two different optical links have been developed for the Level-1 Muon Barrel.
- POLAR exploits a new parallel architecture, G²LINK follows a classic SerDes approach.
- POLAR offers large bandwidth, BIST, parity checks,bus partitioning. It adopts a low-volume, expensive chip-set (1KEuros). Price drops are not expected.

Conclusions @ PDR (2/2) (Nov. 2001)

- G²LINK meets the physical layer specs with a widely used chip-set.
- The two solutions are drop-in compatible, but G²LINK does not offer any data integrity check, which moves into the end-user logic.
- G²LINK tests will include: BER, latency, Synch/Asynch modes, EMI and immunity.

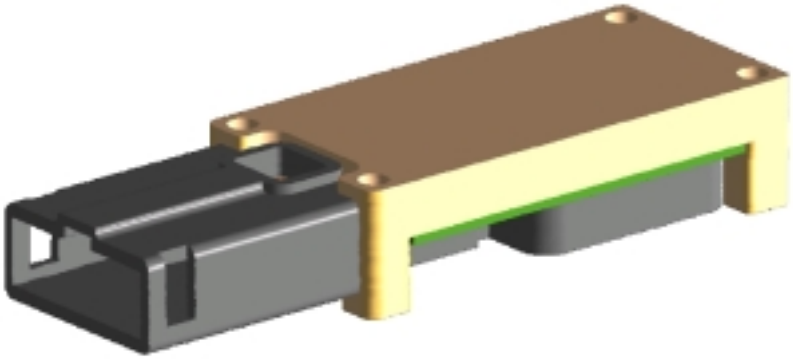
POLAR system



- Parallel optical link based on PAROLI chip-set and XILINX FPGAs
- 48-bit data + 3 strobes @40MHz (>240 Mbyte/s)
- Half-duplex point-to-point architecture with TX and RX nodes
- Fixed low-latency: 220ns @ 10m fiber length

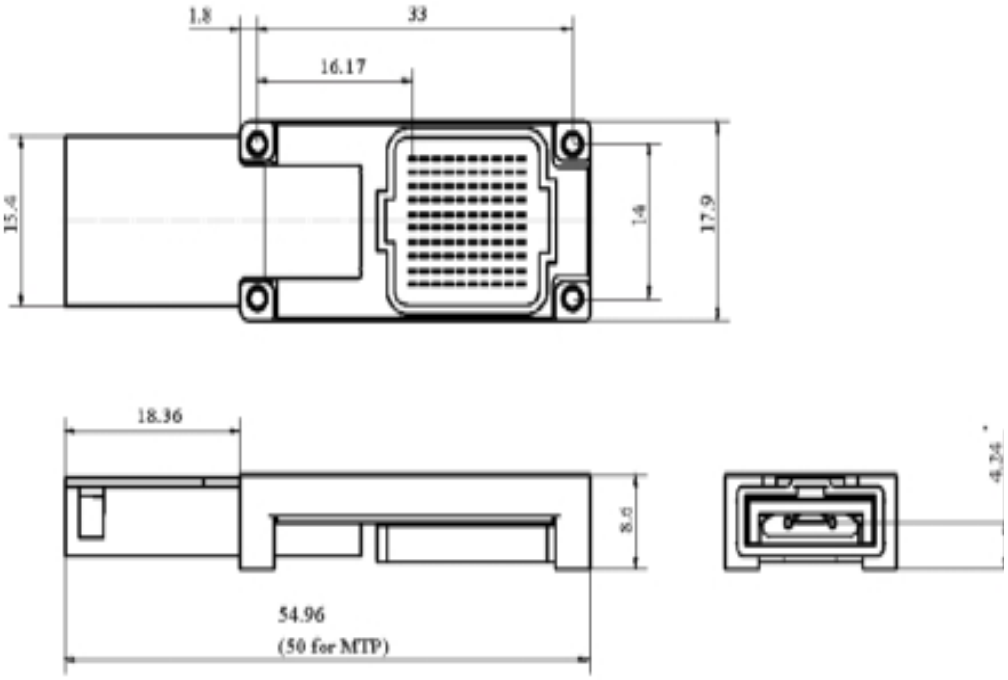
Market trend: PAROLI 2

- Top performances at top price: PAROLI 2



  - Asynchronous, AC-coupled 12 ch. optical link
  - Output power –2 dBm to –7.5 dBm per channel
  - LVDS and CML differential signal electrical interface
  - Transmission data rate of up to 2.5 Gbit/s per channel. 10 Gbit/s per channel planned.

PAROLI 2 - Packaging

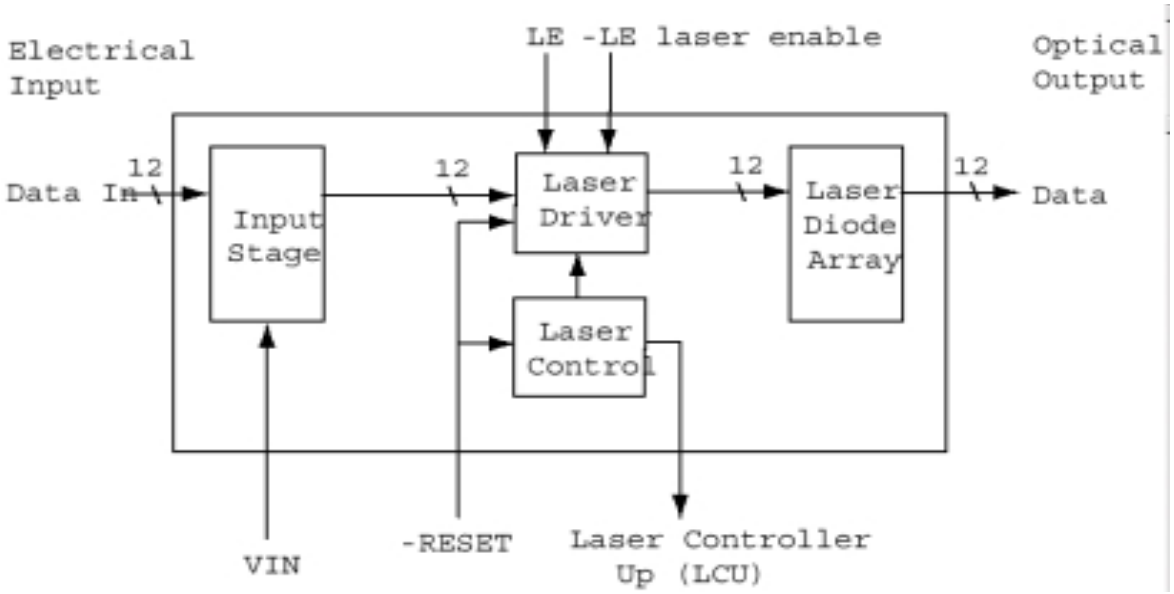


- BGA 10x10 socket
- MTP or SMC optical connector
- Optional customer specific heat sink

PAROLI 2 - TX Specs

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	ICC		350	450	mA
Power Consumption	P		1.2	1.6	W
Data Rate per Channel	DR	(1)		2500	MBit/s



The Serial Approach

- SerDes market is driven by Gigabit Ethernet, FiberChannel, SONET/SDH, etc ..
- Opto devices available both with VCSELs and Lasers.
- OC3 (155Mbit/s), 12 (622Mbit/s), 48 (2.4 Gbit/s) supported. OC192 (10 Gbit/s) sampling now.
- Multisource agreements for SFF Transceivers
- Drawbacks: higher clock frequency (GHz and beyond).

HFBR-5912E

Agilent Technologies
Inventing the Future

Small Form Factor MT-RJ Fiber Optic Transceivers for Gigabit Ethernet

Technical Data

HFBR-5912E,
850 nm VCSEL
HFCT-5912E,
1300 nm FP Laser

Features

- Compliant with Specifications for IEEE 802.3z/ Gigabit Ethernet
- Multisourced 2 x 5 Package Style with Integral MT-RJ Connector
- Performance
  HFBR-5912E (1000 Base-SX)
  - 220 m Links in 62.5/125 µm MMF 160 MHz*km Cables
  - 275 m Links in 62.5/125 µm MMF 200 MHz*km Cables
  - 500 m Links in 50/125 µm MMF 400 MHz*km Cables
  - 550 m Links in 50/125 µm MMF 500 MHz*km Cables

  HFCT-5912E (1000 Base-LX)
  - 550 m Links in 62.5/125 µm MMF Cables
  - 10 km Links in 8/125 µm SMF Cables
- IEC 60825-1 Class 1/CDRH Class 1 Laser Eye Safe
- Single +3.3 V Power Supply Operation with PECL Logic I/O Interfaces, TTL Signal Detect and Transmit Disable
- Wave Solder and Aqueous Wash Process Compatible

Applications

- Switch to Switch Interface
- Switched Backbone Applications
- High Speed Interface for File Servers
- High Performance Desktops

Related Products

- Physical Layer ICs Available for Optical or Copper Interface (HDMP-1636A/ 1646A)
- Quad SERDES IC Available for High Density Interfaces (HDMP-1680)
- 1x9 Fiber Optic Transceivers for Gigabit Ethernet (HFBR/HFCT-53D5)
- Gigabit Interface Converters (GBIC) for Gigabit Ethernet
  SX – HFBR-5601
  LX – HFCT-5611

Description

The HFBR/HFCT-5912E transceiver from Agilent allows the system designer to implement a range of solutions for multimode and single mode Gigabit Ethernet applications.

The transceivers are configured in the new multisourced industry standard 2 x 5 dual in-line package with an integral MT-RJ fiber connector.

Transmitter Section

The transmitter section of the HFBR-5912E consists of an 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) in an optical subassembly (OSA), which mates to the fiber cable. The HFCT-5912E incorporates a 1300 nm Fabry-Perot (FP) Laser designed to meet the Gigabit Ethernet LX specification. The OSA is driven by a custom silicon bipolar IC which accepts differential PECL logic signals (ECL referenced to a +3.3 V supply) and provides bias and modulation control for the laser.

Receiver Section

The receiver of the HFBR-5912E includes a GaAs PIN photodiode mounted together with a custom, silicon bipolar transimpedance preamplifier IC in an OSA. This OSA is mated to a custom silicon bipolar circuit that provides post-amplification and quantization. The HFCT-5912E utilizes an InP PIN photodiode in a similar configuration.

The post-amplifier also includes a Signal Detect circuit which provides a TTL logic-high output upon detection of an optical signal.

- 1.25 Gbit/s transceiver for Gigabit Ethernet
- 850 nm VCSEL, 220m (min) link length
- 3.3V - 0.25A (RX typ), 0.2A (TX typ)
- PECL I/O
- Multi-sourced package
- MTRJ fiber connector

Glink Chip-set

Agilent HDMP-1032/1034 Transmitter/Receiver Chip Set

Data Sheet

1.4 GBd Transmitter/Receiver Chip Set with CIMT Encoder/Decoder and Variable Data Rate.

Description

The HDMP-1032 transmitter and HDMP-1034 receiver are used together to build a high-speed data link for point-to-point communication. These silicon bipolar transmitter and receiver chips are housed in standard plastic 64 pin PQFP packages.

From the user's viewpoint, these products can be thought of as a "virtual ribbon cable" interface for the transmission of data and control words. A parallel word loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel and is then reconstructed into its original parallel form. The channel can be either a coaxial copper cable or optical link.

The chip set hides from the user the complexity of encoding, multiplexing, clock extraction, demultiplexing and decoding. The CIMT encoding scheme used ensures the DC balance of the serial line. When data or control words are not being sent the transmitter sends idle words.

The serial data rate of the Tx/Rx link is selectable in three ranges and extends from 168 to 1120 Mbit/s. This translates into an encoded serial rate of 280 to 1400 MBaud. The parallel data interface is 16 bit TTL. A flag bit is also present and can be used as an extra 17th bit under the user's control. This bit can be used as an even or odd word indicator for dual-word transmission. The encoding of the flag bit can be scrambled to reduce the probability of erroneous word alignment.

A user control space is also provided. If TXCNTL is asserted on the Tx chip, the least significant 14 bits of the data will be sent and the RXCNTL line on the Rx chip will indicate the data is a Control Word.

At the Rx, the PASS feature allows the recovered words to be checked out with the local

Features

- 3.3 V supply, low power dissipation 550 mW Tx, 660 mW Rx
- On-chip encode/decode using Conditional Inversion Master Transition (CIMT) protocol
- 1/N broadcast ready configurable receiver inputs allow multi-point data broadcast using a single transmitter
- Parallel Automatic Synchronization System (PASS) allows receiver to read recovered words with local reference clock
- Robust simplex mode
- Wide range serial rate 280-1400 MBaud (user selectable)
- 5 V tolerant TTL interface 16 or 17 Bits wide
- Low cost 64 pin plastic package 10x10 mm² PQFP

Applications

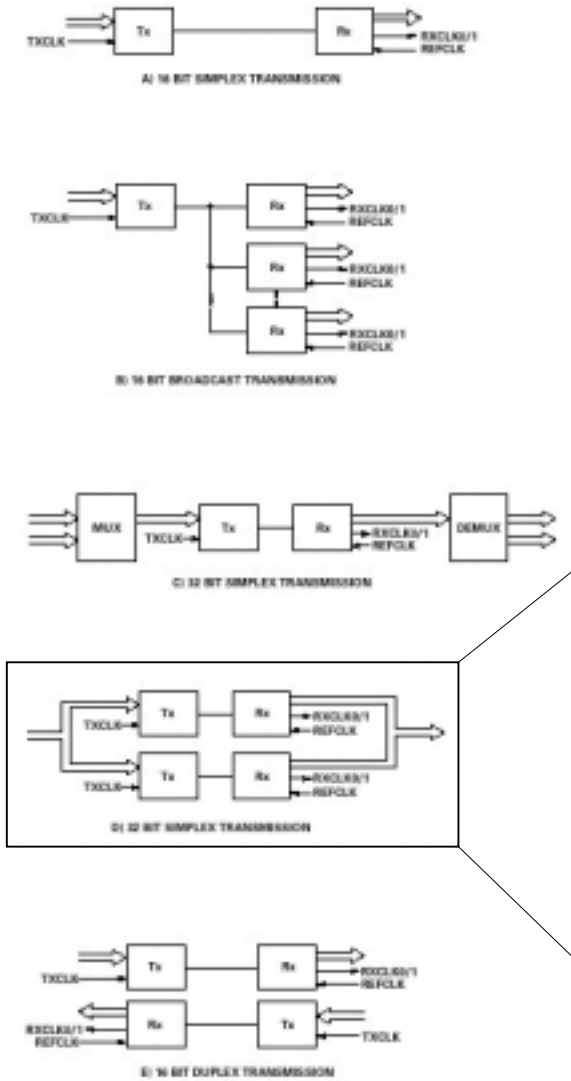
- Cellular base stations
- ATM switch
- Backplane/bus extender
- Video, image acquisition
- Point to point data link
- Implement SCI-FI standard

Agilent Technologies

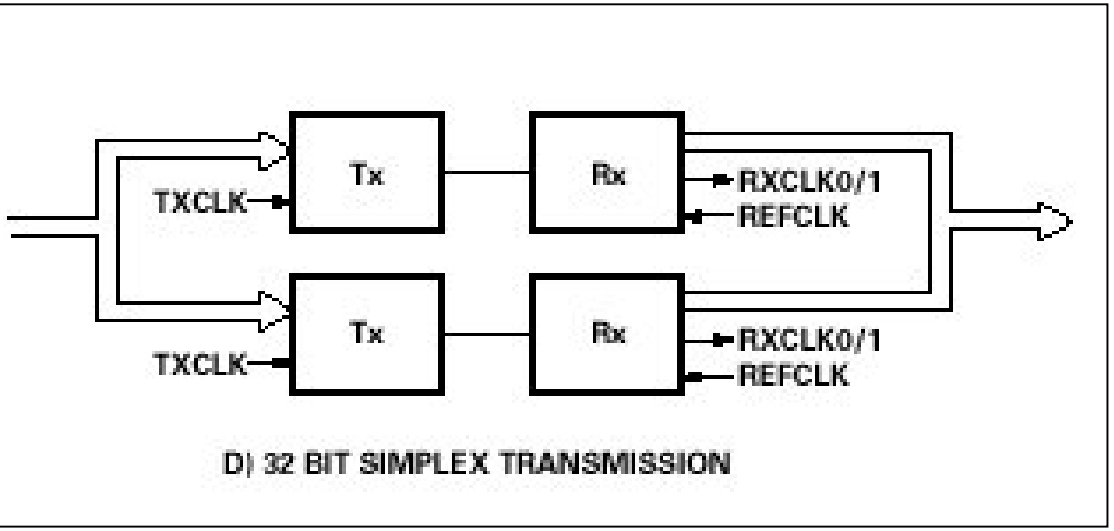
Innovating the HP Way

- Third generation GLink chip-set (HDMP-103x)
- 3.3V – 660 mW (RX typ), 590 mW (TX typ)
- TTL for parallel I/O, PECL for serial I/O
- 16 + 1 bit data size
- Single source, but strongly supported by Agilent

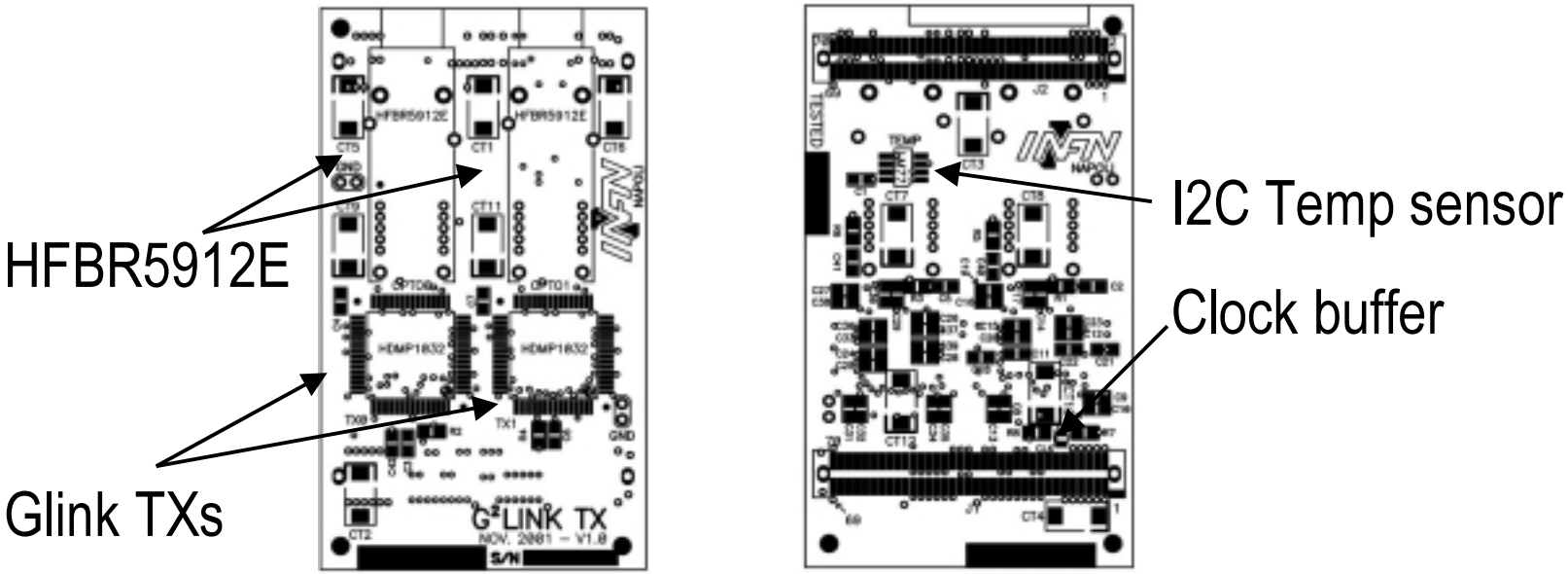
G²LINK => Dual GLink



- Two channels are required to transmit 32 bit words @ 40 MHz
- Separate paths for trigger and data

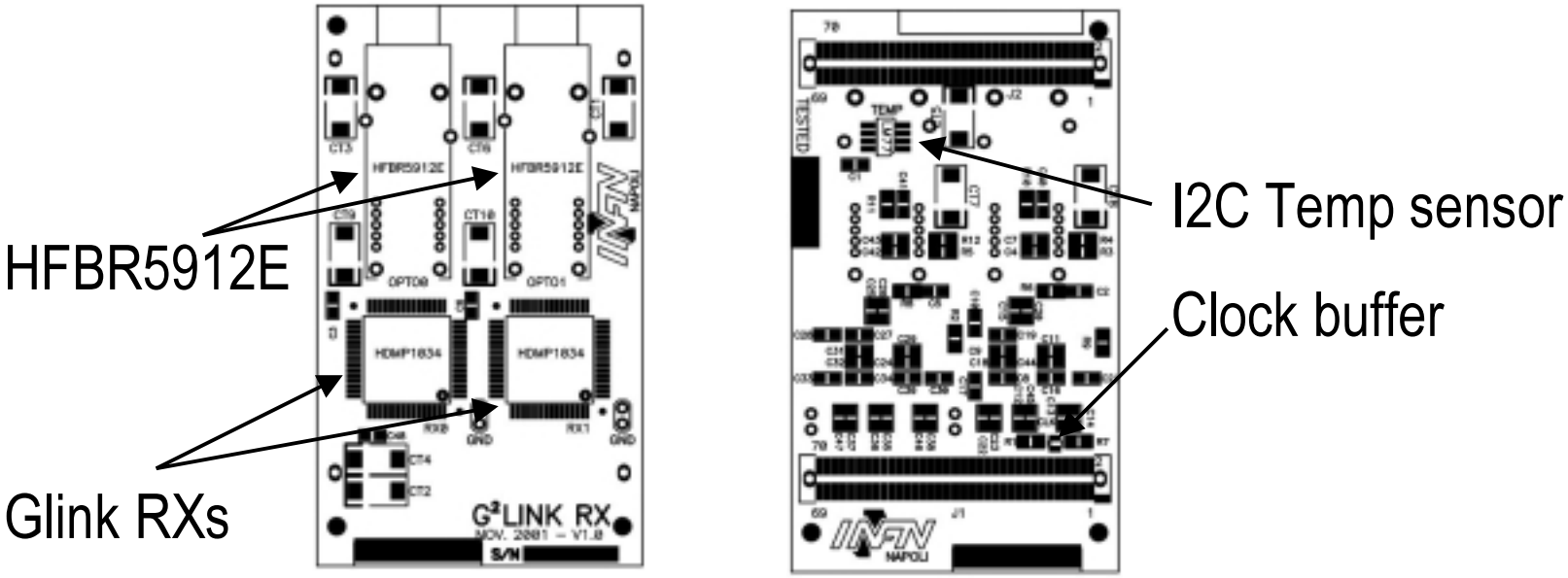


G²LINK TX



- Drop-in replacement for POLAR TX: form factor and connectors pin-to-pin compatible
- 10 layer PCB with controlled line impedance
- Split power planes for noise immunity

G²LINK RX



- Almost pin-to-pin compatible with POLAR RX
  Minor changes required to the user's logic
- 10 layer PCB with controlled line impedance.
- Split power planes for noise immunity.

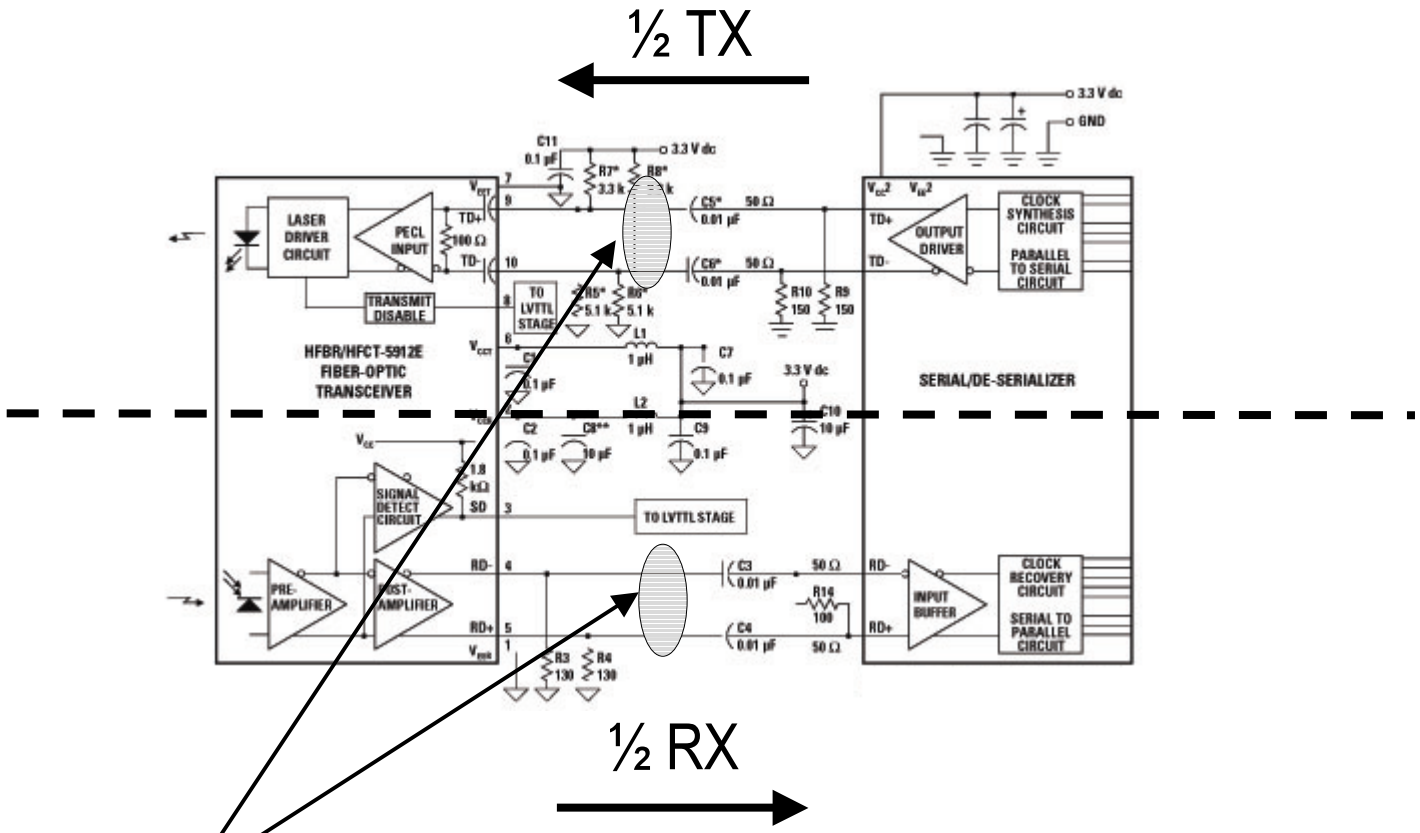
G²LINK Status @ PDR

- PCBs are ready and impedance of critical nets has been already characterised with TDR techniques.
- Board assembly is started.
- The POLAR test bench will be used with minor changes to qualify also G²LINK.
- Preliminary test results will be available before the end of the year.

G²LINK Status @ FDR

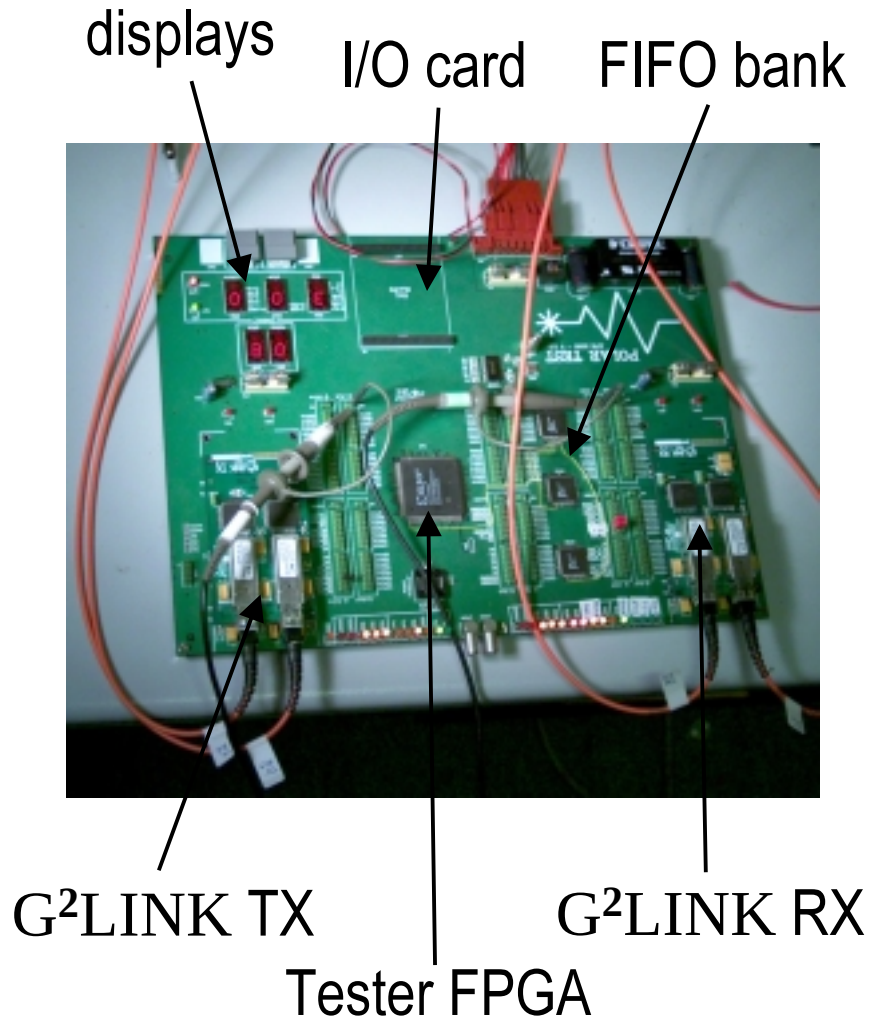
- Five TX and RX nodes have been assembled and fully tested
- Backward compatibility with POLAR verified on the field

G²LINK Block Diagram



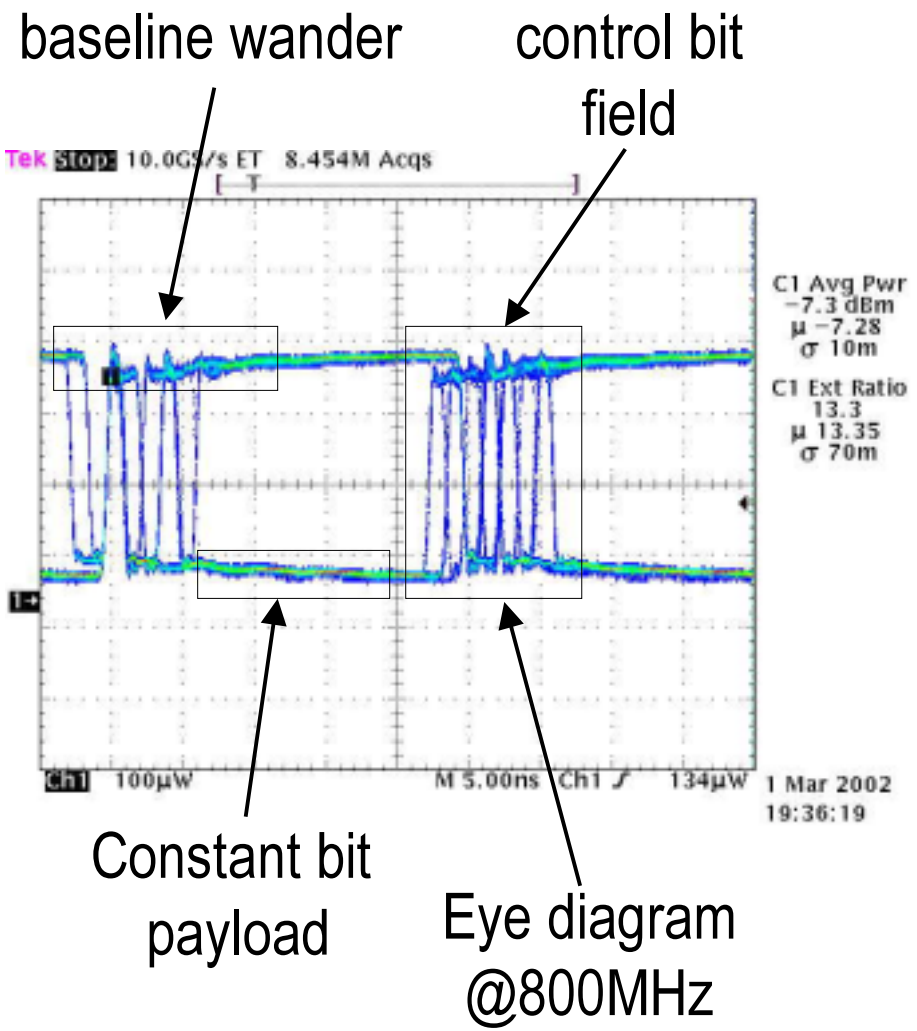
- 800 Mbaud (20x) serial data rate
- AC coupled, 100 Ohm terminated, diff. PECL

Testing G²LINK



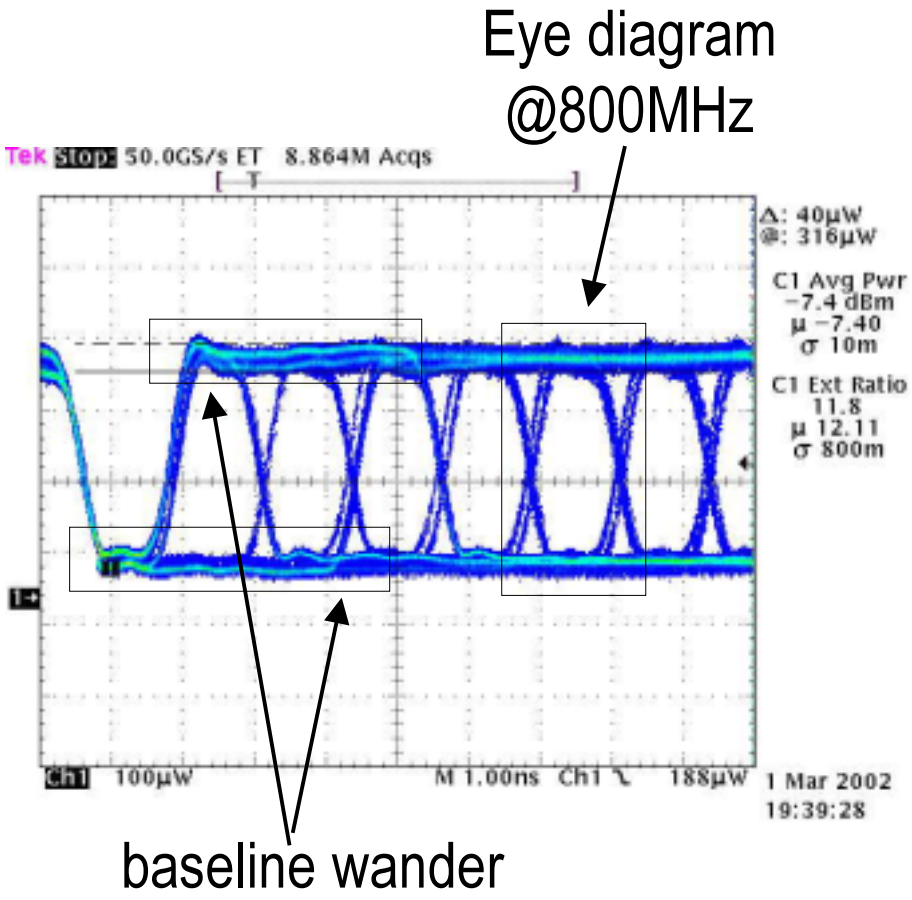
- To test the link, we used the custom parallel Bit Error Rate tester designed for POLAR
- The Tester FPGA checks the received data against the transmitted patterns
- Data and protocol errors are displayed
- No errors detected in 4 weeks of continuos operations

Test Results - 1



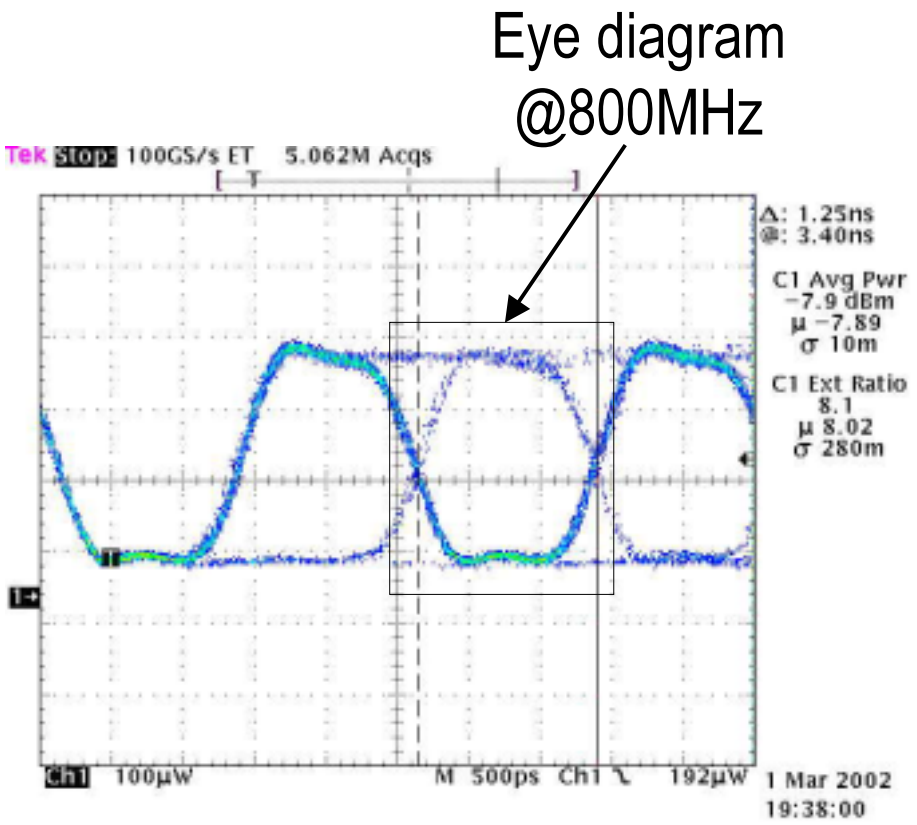
- Constant bit payloads (all 0s, all 1s sequences) stress the Clock Detection and Recovery circuitry (min transition density)
- Analysis of control bit fields using eye diagram at max toggle rate (800MHz)
- Worst case baseline wander

Test Results - 2



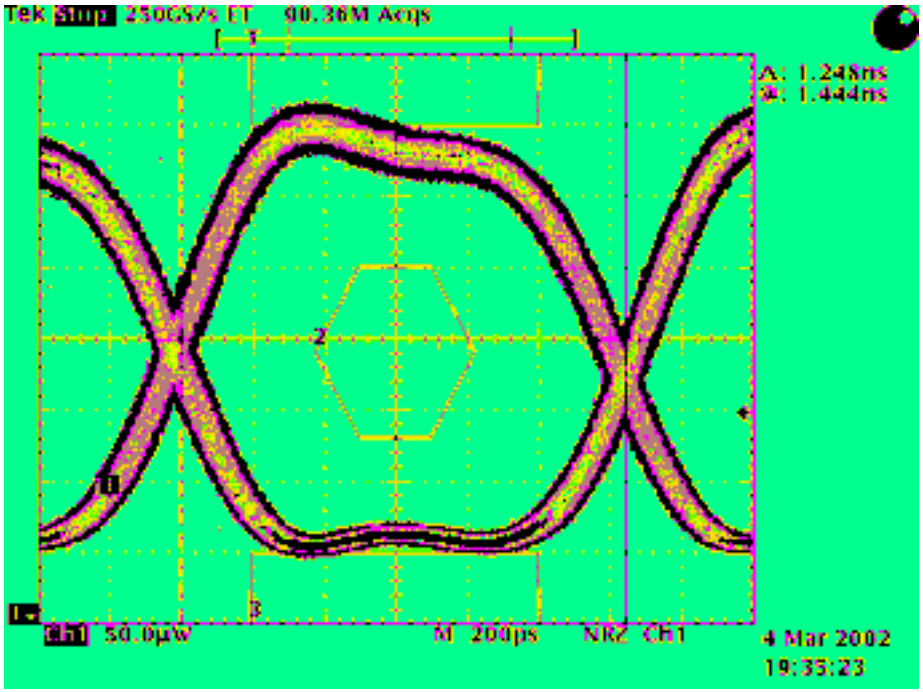
- Alternate bit payloads (A/5 sequence) guarantee the highest transition density
- Eye diagram @800 MHz in the payload
- Minimize baseline wander

Test Results - 3



- Low transition density payloads are characterized with walking one, walking zero sequences.
- Eye diagram at max toggle rate with low baseline wander.

Test Results - 4



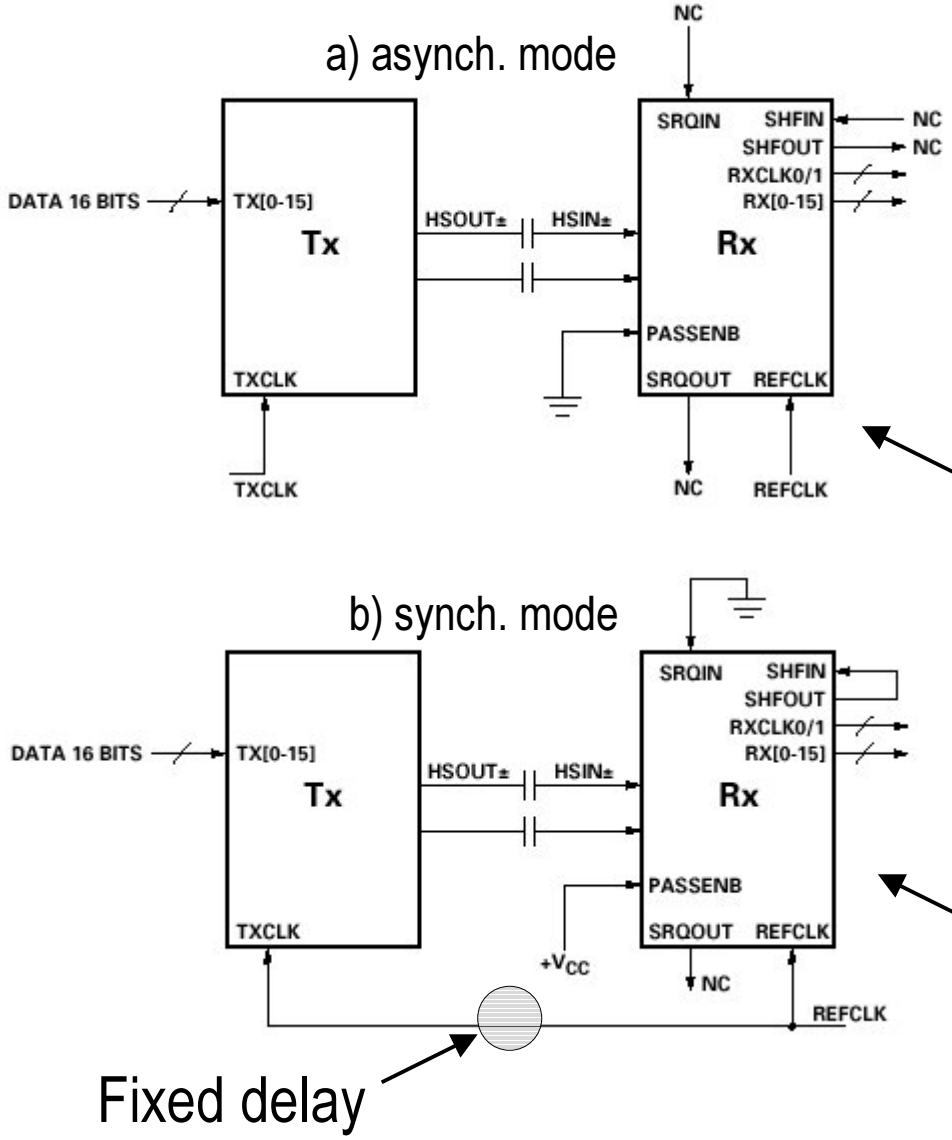
- Eye diagram with GB Ethernet (1.25 Gbit/s) mask shows excellent behavior.
- Mask test results are function of many variables:
  - data pattern (A/5)
  - data encoding (NRZ)
  - trigger pattern (01110)

Test Results - 5

Current @ 3.3V

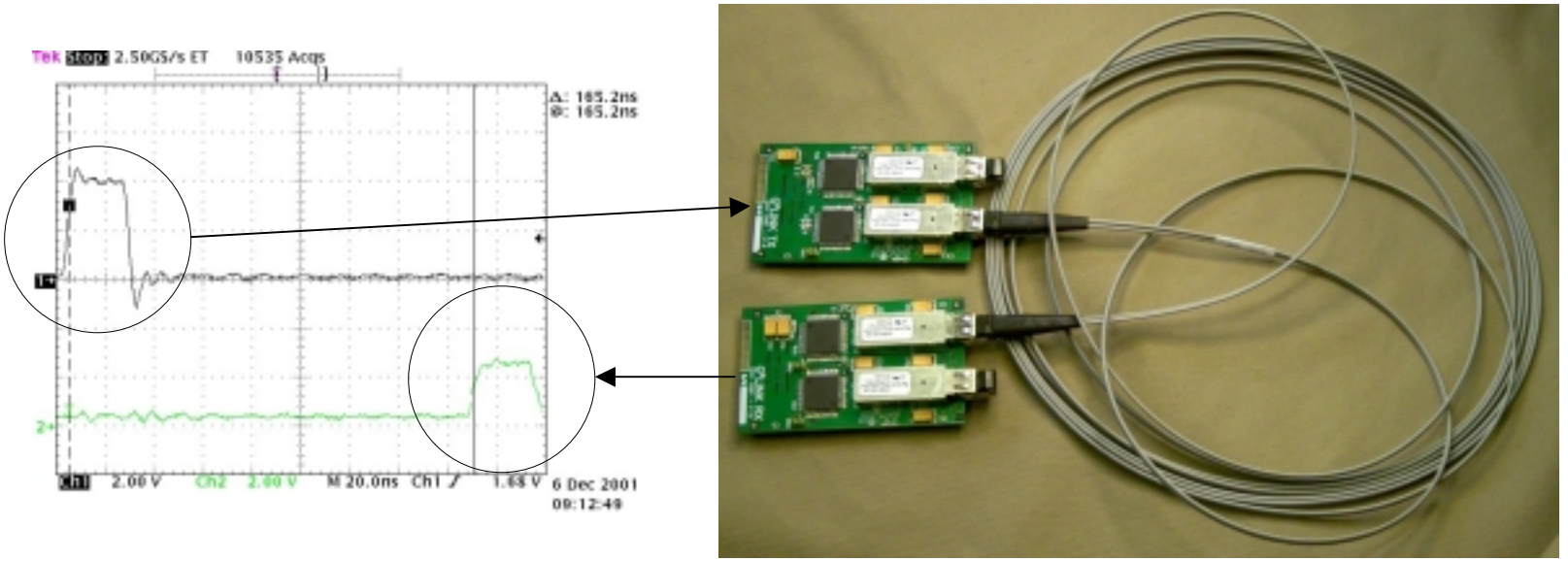
Sequence	TX (mA)	RX (mA)
0/F	460	680
A/5	460	690
W0	450	600
W1	460	670

Asynch vs. synch architecture



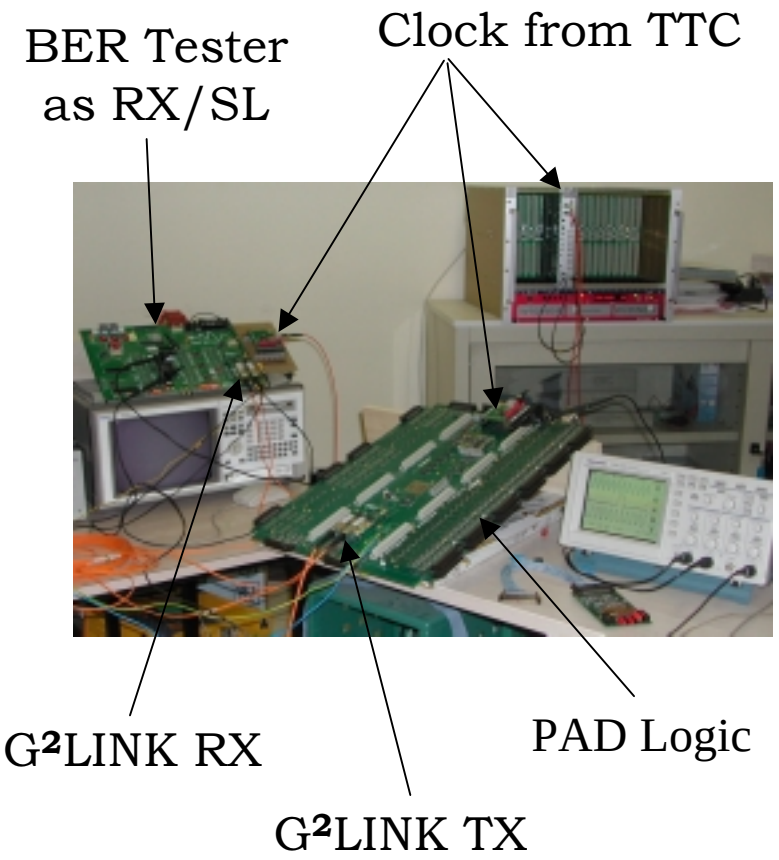
- G²LINK supports both Asynch and Synch mode of operations.
- In Asynch mode, RX clock has no phase relatioship to the TX clock.
- In Synch mode, TX and RX clocks are phase-locked.

Link Latency in Synch Mode



- In Synch Mode TX and RX clocks are derived from the same source
- Link latency is 165ns @ 10m fiber length

PAD to ROD emulation



- PAD to ROD (10m) data transfer has been tested in Rome using G²LINK and TTC clock distribution
- RX/SL is emulated by the BER Tester. Its internal oscillator is disabled and an external TTC generates the reference clock.
- G²LINK is configured in Synch mode
- No errors have been observed

RAD Tests

- Gamma irradiation has been conducted by the TGC community at the Co^{60} facility of RCNST, University of Tokyo. From H. Hasuko, “Preliminary Report on TGC RHA Test”, Dec.2001:
  - …”First, a GLINK board was tested. It consists of a set of EO/OE converter,GLINK 1032/1034 rx and tx. During the irradiation, the board was biased.Total Vcc current of the set was monitored and logged by a DMM with a PC.A local control/monitor (LCM) system has been built for the test.The LCM sent 16-bit test patterns (0x5555 and 0xaaaa) at 40 MHz to the GLINK rx via OE conversion; received data directly went to the GLINK tx on the board and were sent back to the LCM by EO conversion.The consistency of the data were checked there. All the link error signals were also monitored and logged by the LCM.A LVDS board was also tested. We had no error for both GLINK and LVDS during the irradiation. **No data inconsistency was observed; no link errors occurred**. The total current is stable and no significant increase was observed…” ...

Costs

■ HFBR-5912E	100	Euro (x 2)
■ HDMP-103x	50	Euro (x 2)
■ Connector	10	Euro (x 2)
■ Clock Buffer	1	Euro
■ Temp Sensor	2	Euro
■ Passive	20	Euro
■ PCB	15	Euro
■ Assembly	20	Euro
■ Total (per each node)	378	Euro + VAT

Conclusions (1/2)

- G^2Link passed all the tests in our Electro/Optical qualification program:
  - BER, Optical Eye Diagram, Baseline wander
  - Latency and Synch Mode test
  - TTC clocking scheme
  - PAD Logic integration
- Gamma Test has been successfully passed (see H. Hasuko *et al.*). Neutron test is planned.
- Still to be done: PRBS test, long-fiber run, EMI

Conclusions (2/2)

- In the present scenario, PAROLI is tailored for extreme performance architectures, where price is not an issue.
- G2LINK meets all the specs, offering reliable operations at a reasonable price.
- New silicon (HDMP-103xA) is now available from Agilent
- The actual design can be easily modified to implement a 16-bit full-duplex link.