Bus in a new light

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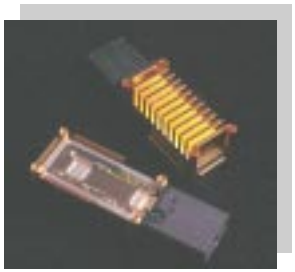
Overview

We describe a parallel optical link based on the SIEMENS' PAROLI DC chipset - a 22 bit optical parallel bus.
The interface to the link has been designed around XILINX FPGAs, in order to transmit 32 bit data plus 4 bit flags at 40MHz with parity check. The FPGA design handles the user payload at 40 MHz and performs segmentation and reassembly at 200 MHz .
In this work, emphasis is put on the FPGA interface to the SIEMENS' chip-set - a design which puts to the proof the FPGA architecture.
We also present POLAR, a VME board which implements a full-duplex parallel optical link using this architecture:

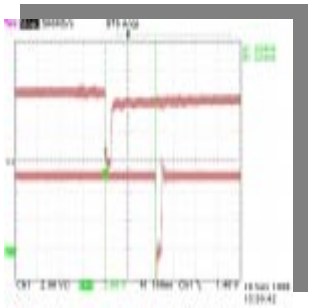
bus in a new light ...

Road map

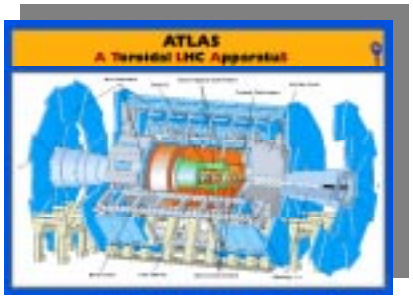
- PAROLI chip-set: how it works



- The POLAR board: A Parallel Optical Link ARchitecture
- Link features

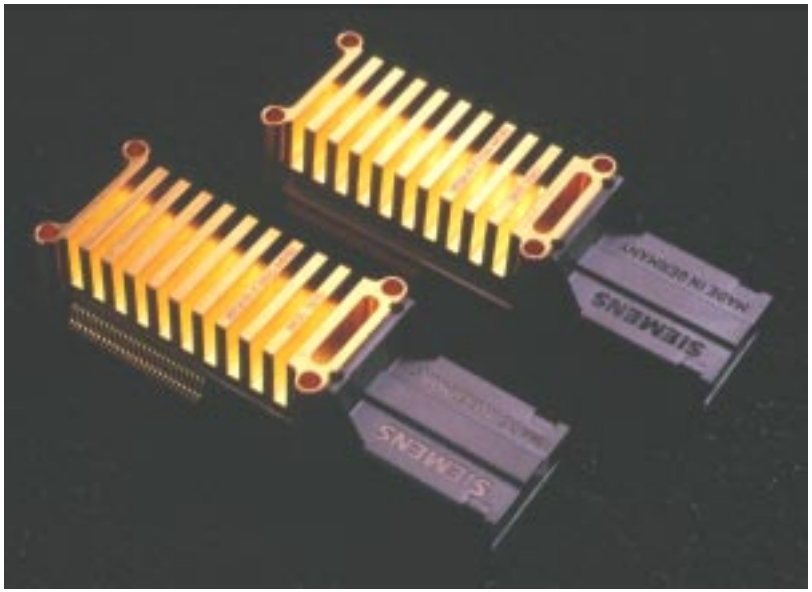


- POLAR in the ATLAS Experiment



- Conclusions

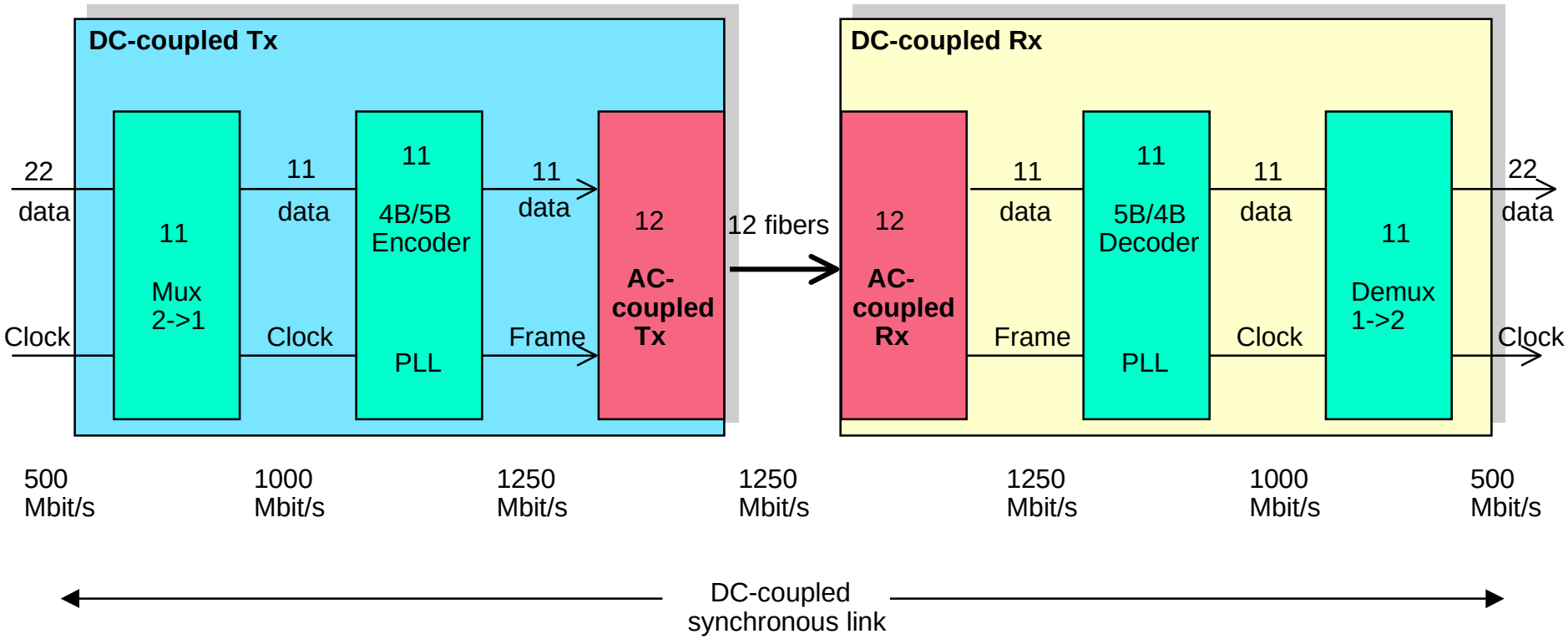
PARallel Optical LInk chip-set



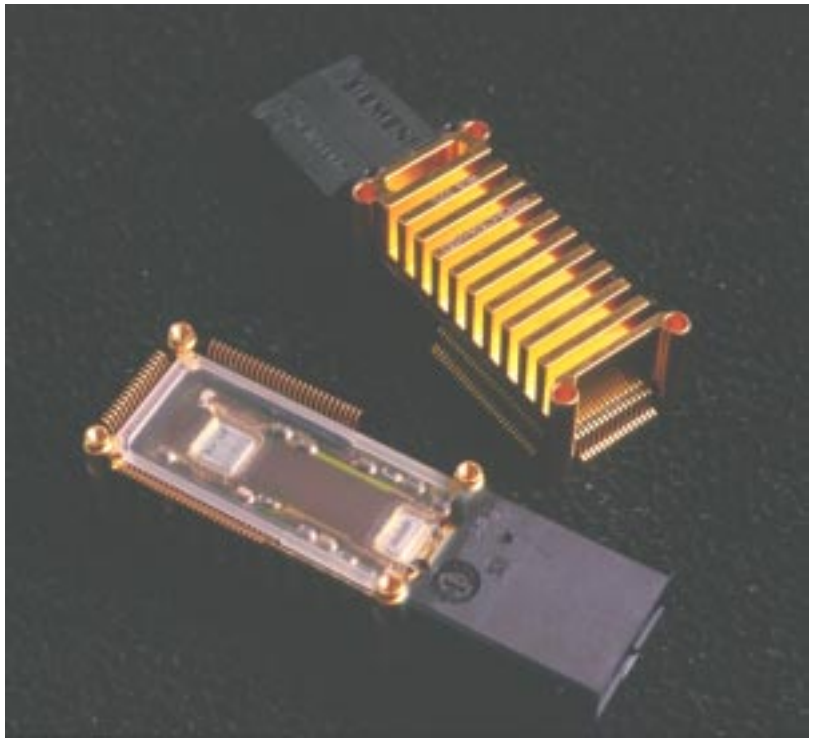
The PAROLI DC chipset is a parallel optical link developed by SIEMENS for high speed data transmission.
The system consists of a TX module, a ribbon of 12 fibers and a RX module.
The PAROLI TX is seen by the user as a parallel 22 bit register, clocked at a frequency which spans from 200 MHz (min) to 500 MHz (max.). It converts the parallel electrical input (data and clock) into a parallel optical output feeding the 12 fiber ribbon. The input data received on the optical interface of the RX module is then converted in a 22-bit parallel word with a clock signal running at the same frequency as the transmitter clock.

PAROLI Block Diagram

Source: SIEMENS



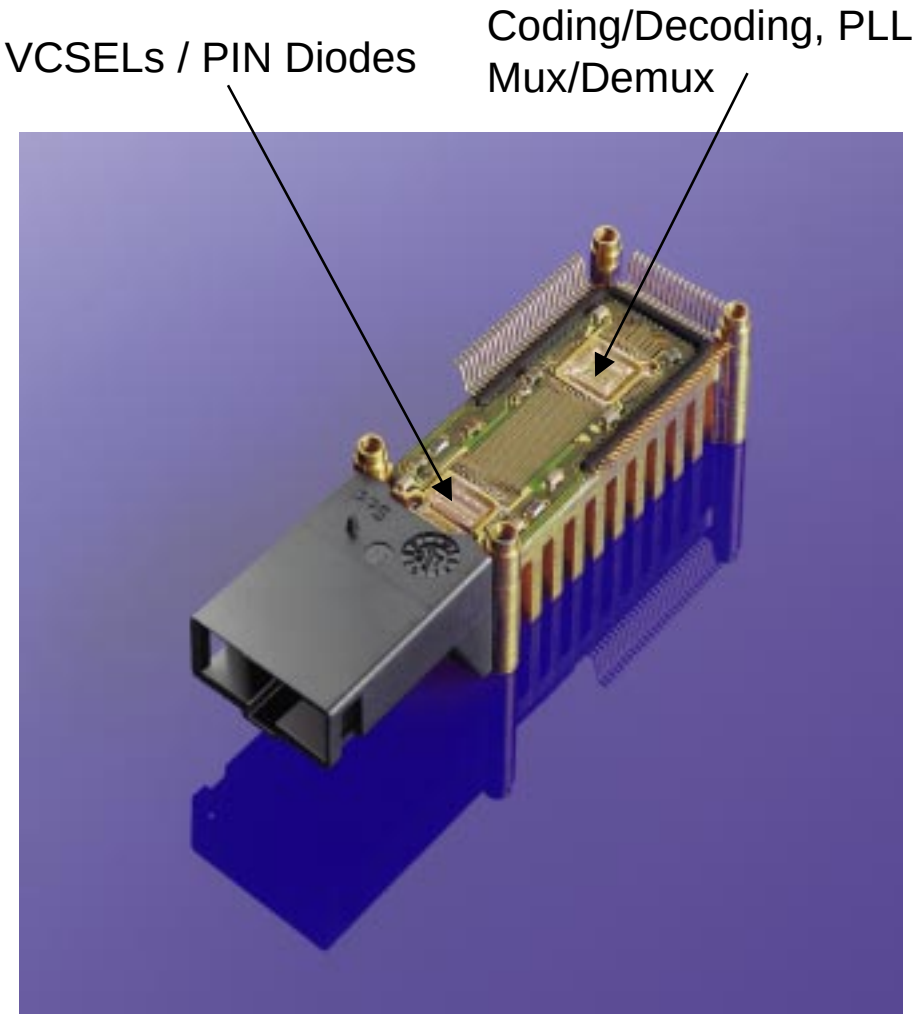
PAROLI Specs (Electrical)



- Package
  - SMD 72 leads, pitch 0.65mm

- Power:
  - 3.3V
  - 1 A (typ)
  - 4 W (max)
- 200 - 500 MHz clock
- Logic levels:
  - LVDS for data and clock
  - LVCMOS for controls

PAROLI Specs (Optical)

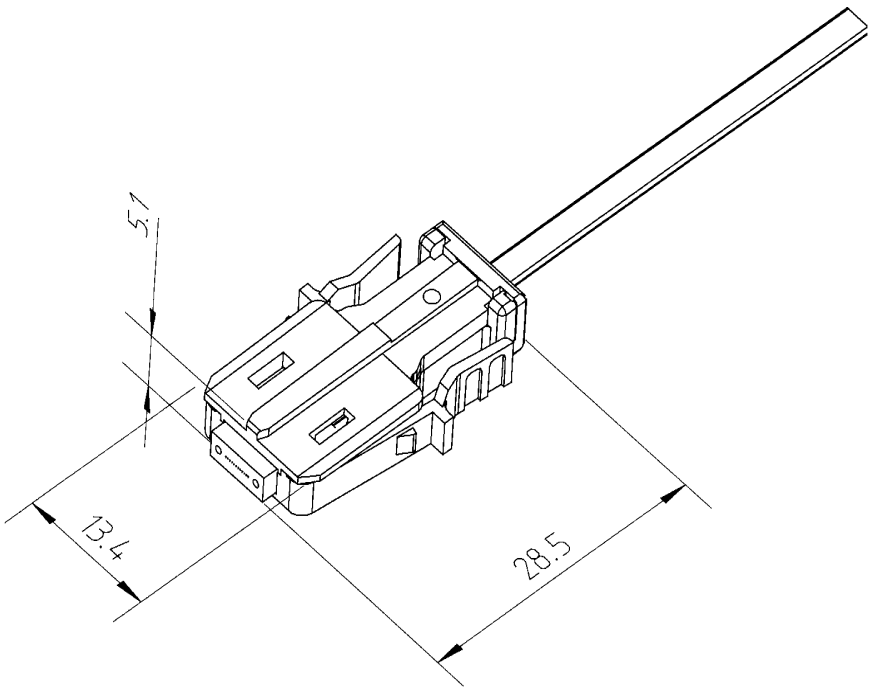


- Tx: 840nm VCSELs
- Rx: 840nm PIN diode array
- Laser safety:
  - Class 1 FDA
  - Class 3A IEC
- Optical data rate:
  - 1.25Gbit/s (max)

Source: SIEMENS

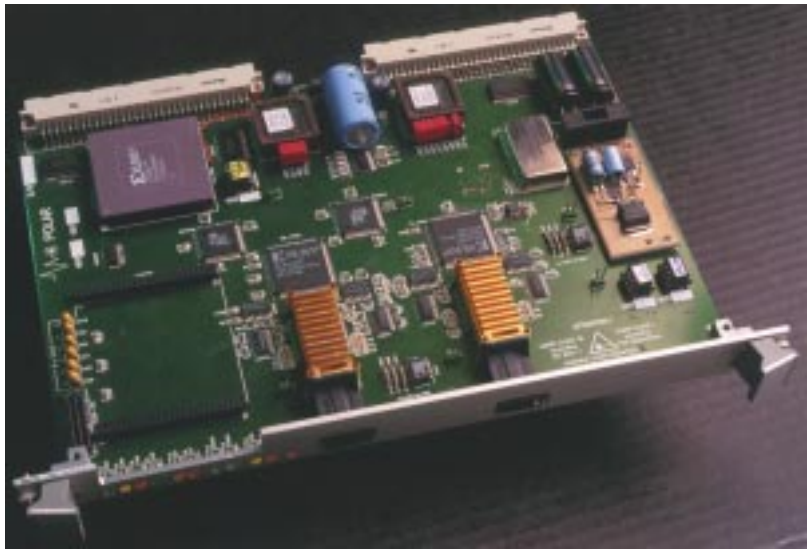
SMC (Simplex MT Connector)

Source: SIEMENS



- design optimized for the PAROLI module:
  - snap-in
  - mechanical keying
- MT compatible:
  - fiber spacing: 250µm
- 12 Fiber ribbon:
  - 62.5 µm graded index multimode fibers

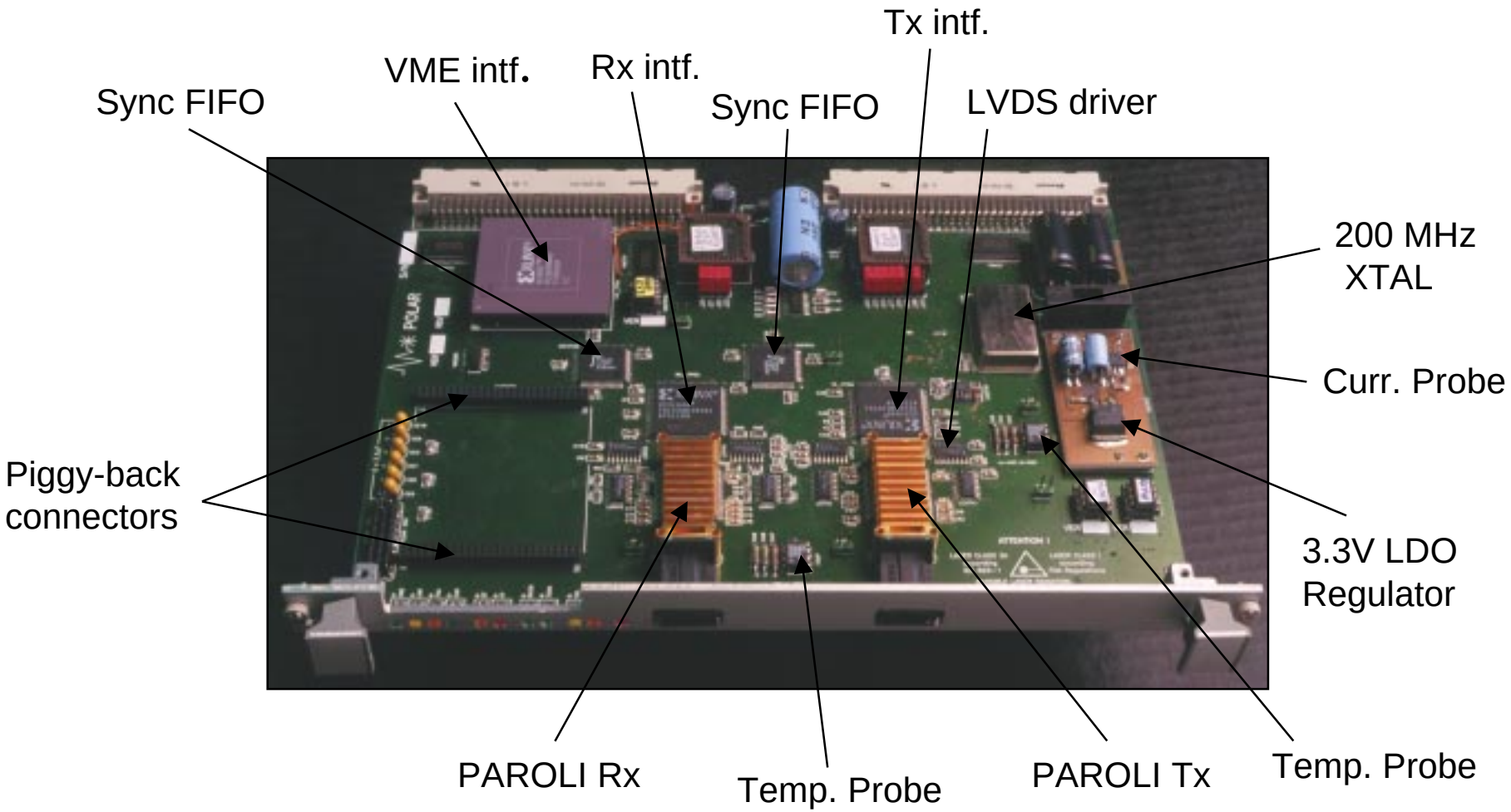
POLAR Board



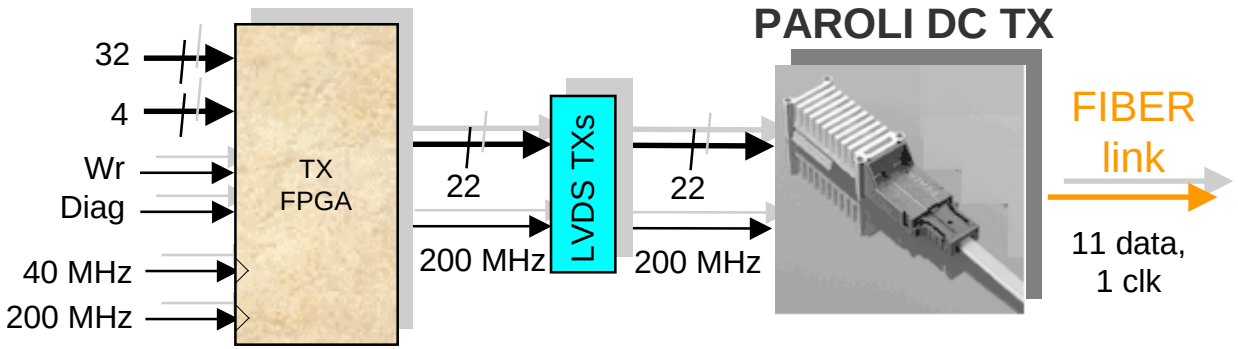
- Full-duplex parallel optical link
- VME 6U board:
  - A32/D32, BLT
- based on PAROLI Tx/Rx

- I/O data rate: 32 bit @ 40 MHz (each way)
- FPGA design running @ 200MHz (5x user-clock)
- Extension Module, Temp. and Current Monitor

POLAR Board (Layout)

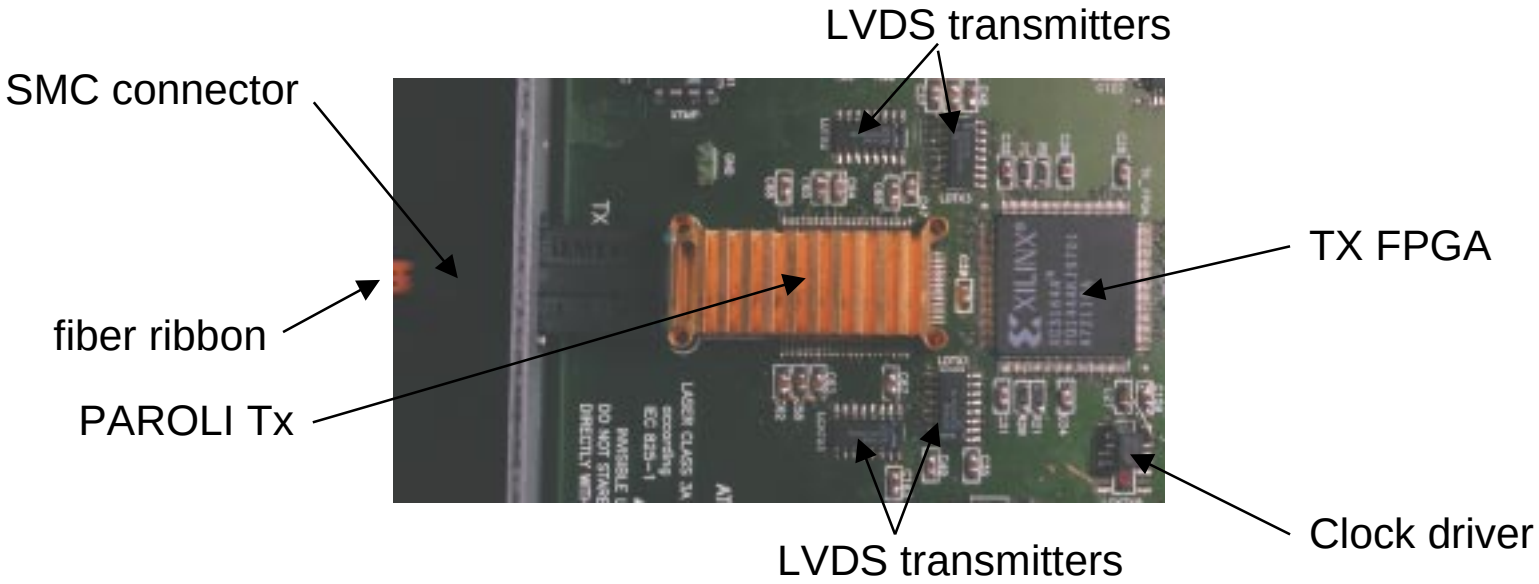


PAROLI Tx interface (block)



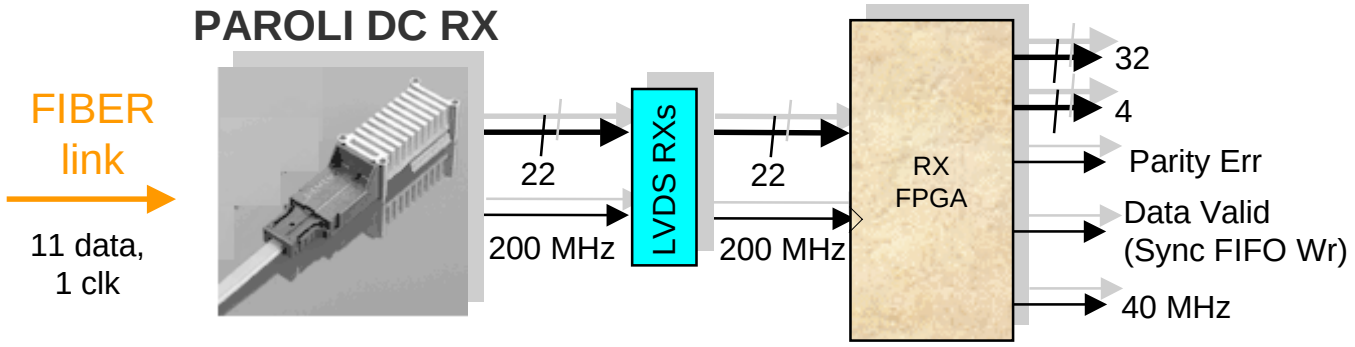
- TX FPGA segments the 32-bit data word in four 16-bit fields: Header, MSword, LSword and Parity
- 4-bit word is also transmitted (user flags)
- Single-word and block transfer (random length) are supported
- Test pattern can be generated in diag mode
- User clock runs @ 40 MHz
- TX FPGA feeds PAROLI with data and clock @ 200MHz

PAROLI Tx interface (layout)



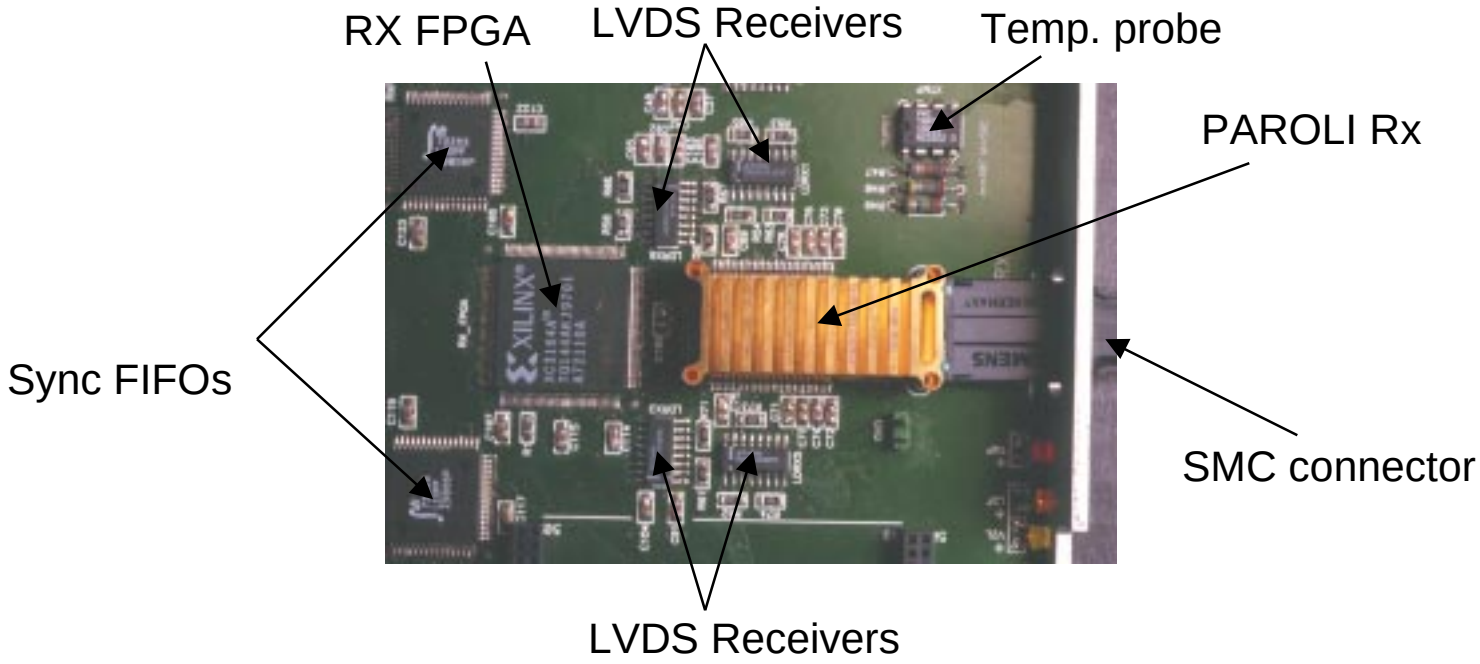
- The TX FPGA performs data framing @ 200 MHz. At this clock frequency, the physical layout plays a key role in determining the digital system performance. Multi-layer boards with multiple ground and VCC planes, controlled line impedance and differential transmission scheme are required to achieve an acceptable signal integrity.

PAROLI Rx interface (block)



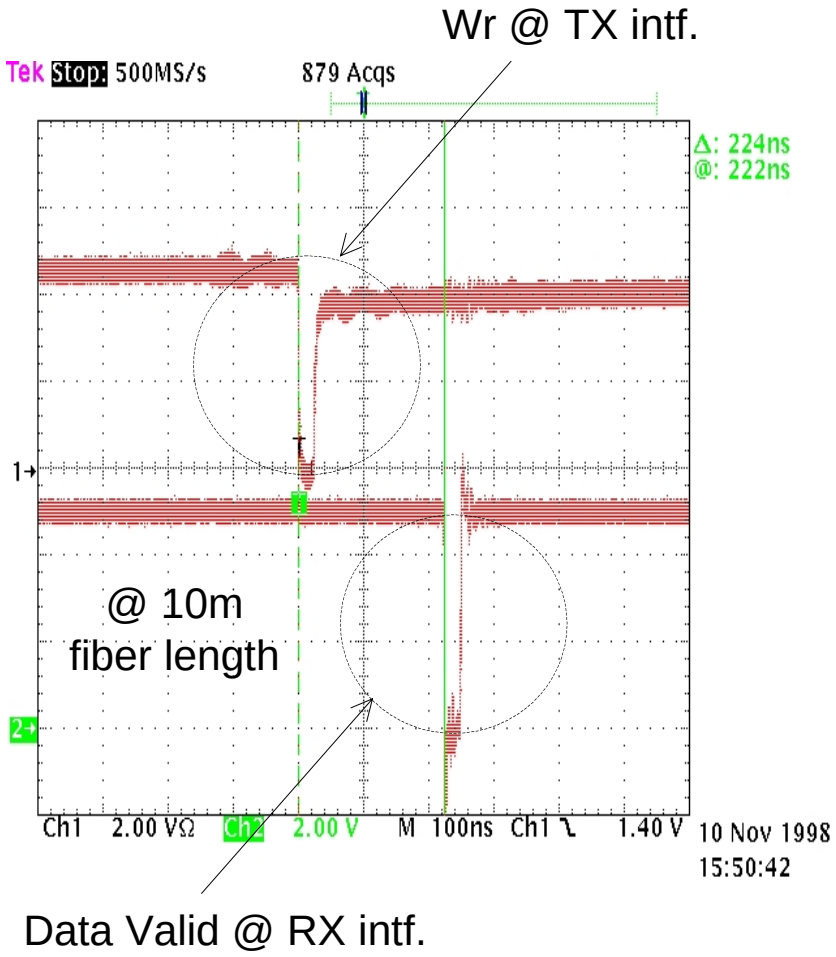
- RX FPGA takes PAROLI data and clock @ 200MHz and reassembles the Header, MSword, LSword fields in a 32-bit data word + 4-bit flag word
- Parity is checked
- 40 MHz clock is recovered
- Data can be written to IDT SyncFIFO @ 40 MHz

PAROLI Rx interface (layout)



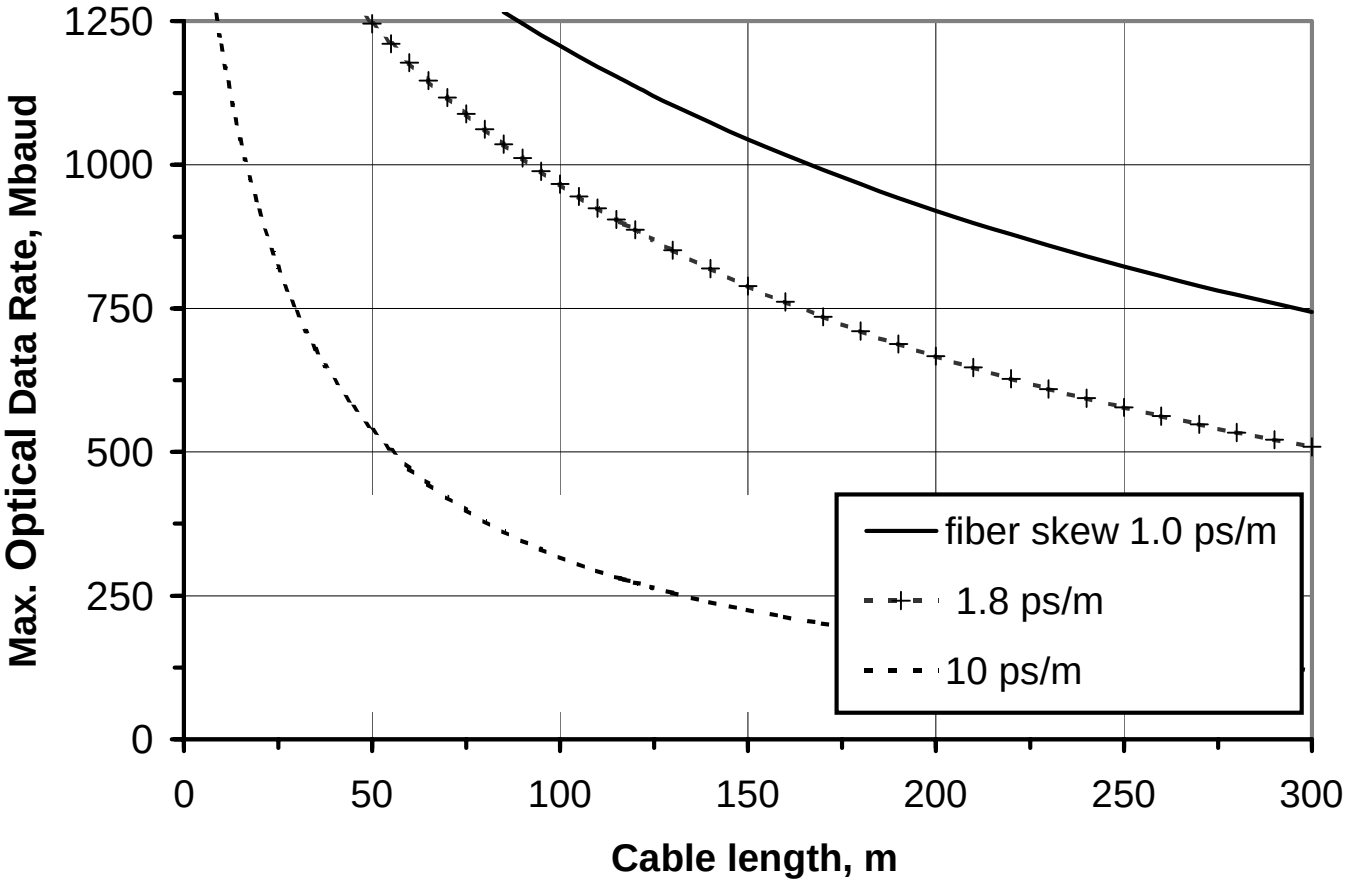
- Analog issues like reflections, ground-bounce and cross-talk are also present in the RX interface. LVDS I/O standard offers low voltage swing (~ 400mV) with low power consumption and EMI.

Link latency



- PAROLI delay is:
  - @ Tx: 4 clock cycle + 3ns
  - @ Rx: 3 clock cycle + 3ns
- Fibers add ~5ns/m
- TX and RX FPGA interfaces need 14 cycles each (in the present design)
- **Link latency is predictable and constant**

Fiber length vs. data rate

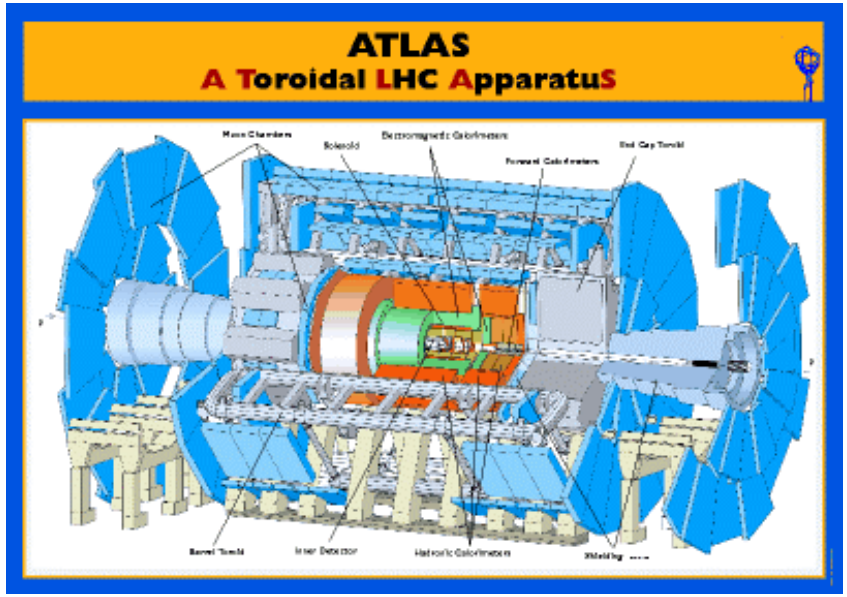


Source: SIEMENS

What's next

- We plan to migrate both Tx and Rx FPGAs from the XC3100A (5V) to the new XC4000XLA (3.3V) family
- Data bus will increase to 40 bits
- The SuperSync FIFOs (IDT) will be replaced by the new SuperSync II family which offers faster speed grades and higher densities @ 3.3V

POLAR in the ATLAS Experiment



- POLAR has been proposed to the ATLAS collaboration at CERN. Presently this optical link is under evaluation in view of its utilization in the Muon Trigger and RPC read-out

- The fixed latency shown by POLAR allows using it in trigger architectures, where timing performances are at a premium
- Test are scheduled to verify the rad-tolerance of the PAROLI chipset

Conclusions

- PAROLI chip-set allows designing a parallel optical link in the range of GByte/s
- Link latency is constant
- FPGA-based designs can manage a parallel optical link with a data rate of 32 bit@40 MHz
- POLAR shows how the PAROLI chip-set can be embedded in a VME environment