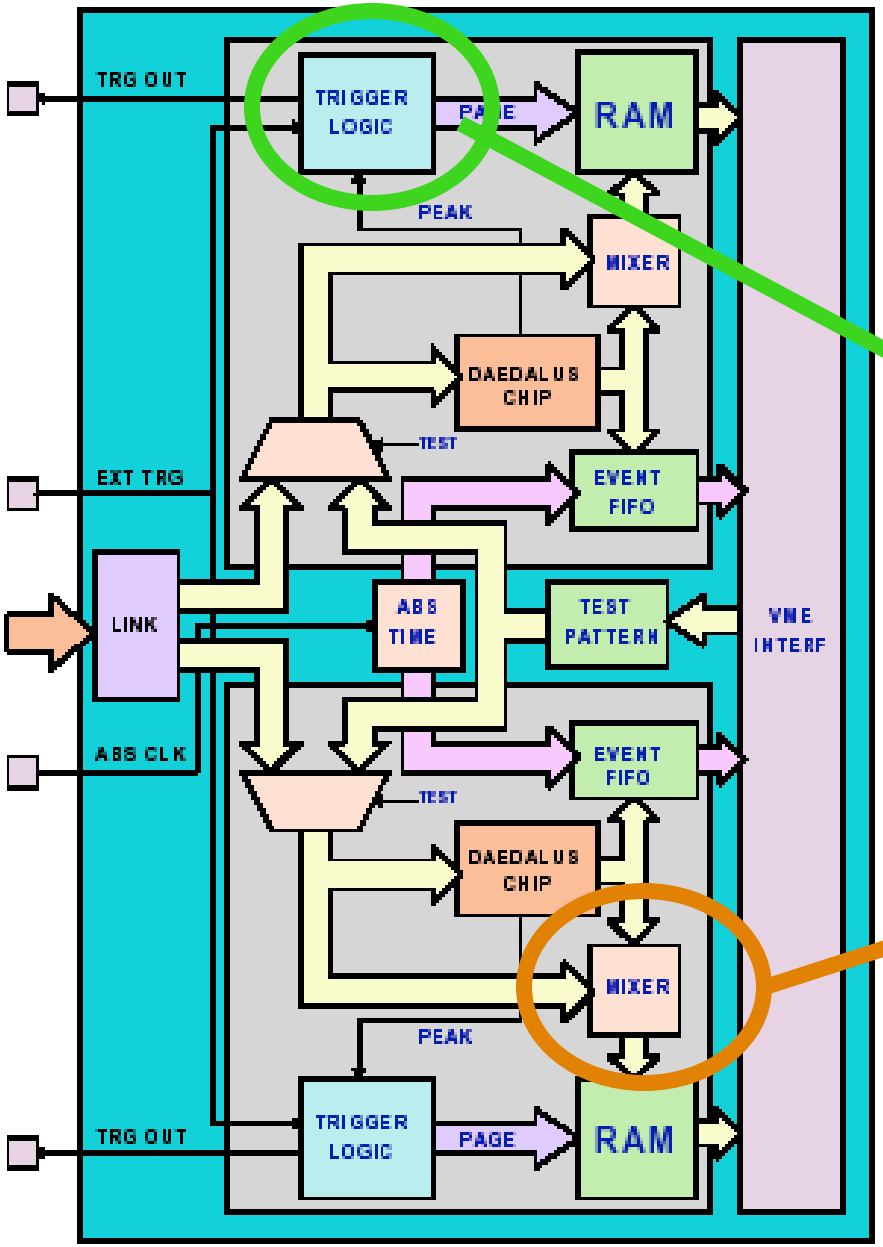
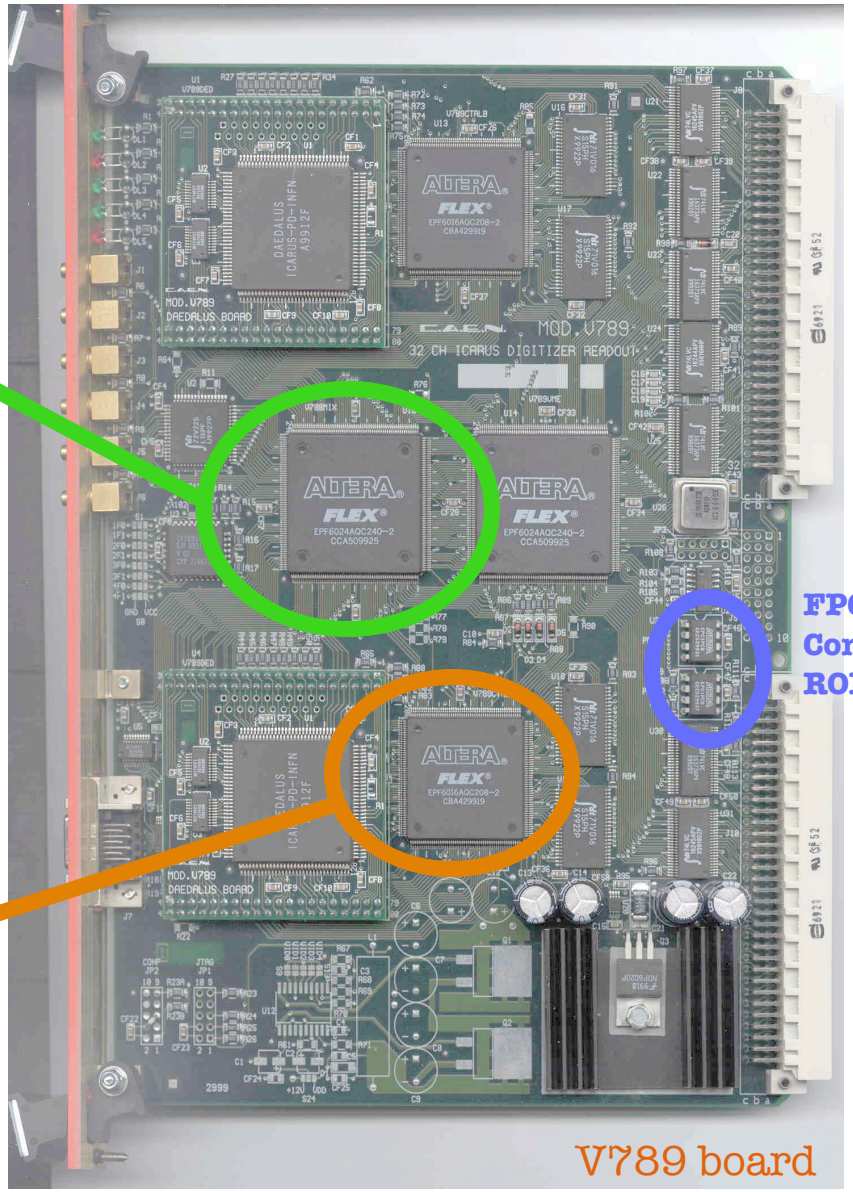
A possible upgrade for the V789 firmware

V789 block diagram





V789 board

A possible upgrade for the V789 firmware

V789 logic implemented on FPGA chips which:

Can be easily reprogrammed (changing the serial rom)

Have quite some free gates (> 50%) to enhance present behaviour

Address those issues:

Data Format in memory buffers

Introducing lossless compression

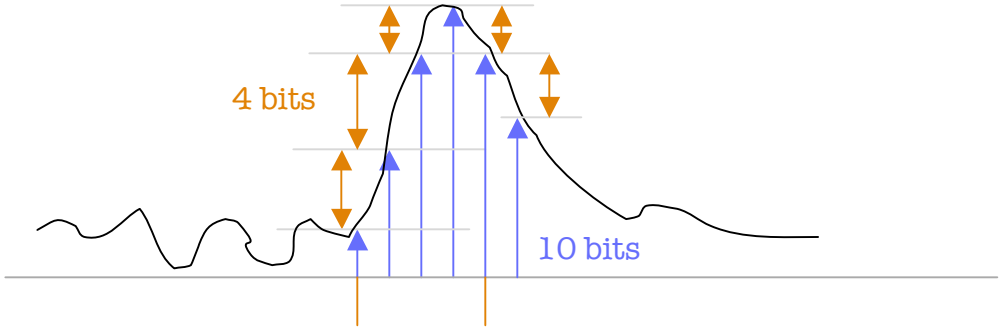
Adding a new parameter in the trigger logic

Enhance Dedalus efficiency discriminating on signal width

Documentation

Present logic is self documented only by Abel source listings (obsolete)

Event Data Format upgrade I



Reducing raw data size using lossless Difference Coded Compression

Compression Algorithm illustrated in may '02

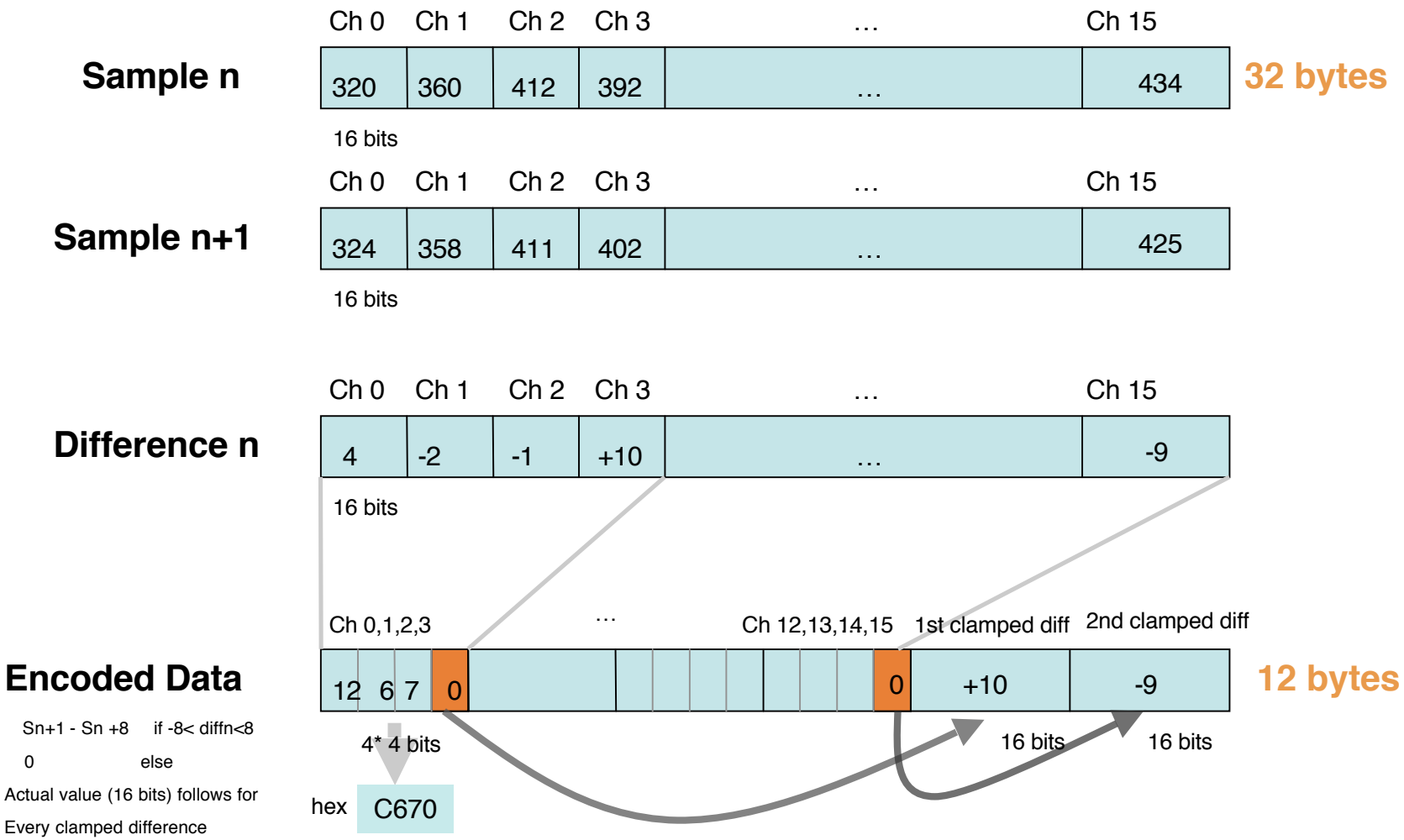
Packs 4 samples in one 16-bits word
Actual compression ratio achieved on raw data ~3.9

Requires Intervention on "Mixer" and "ADGEN" logic

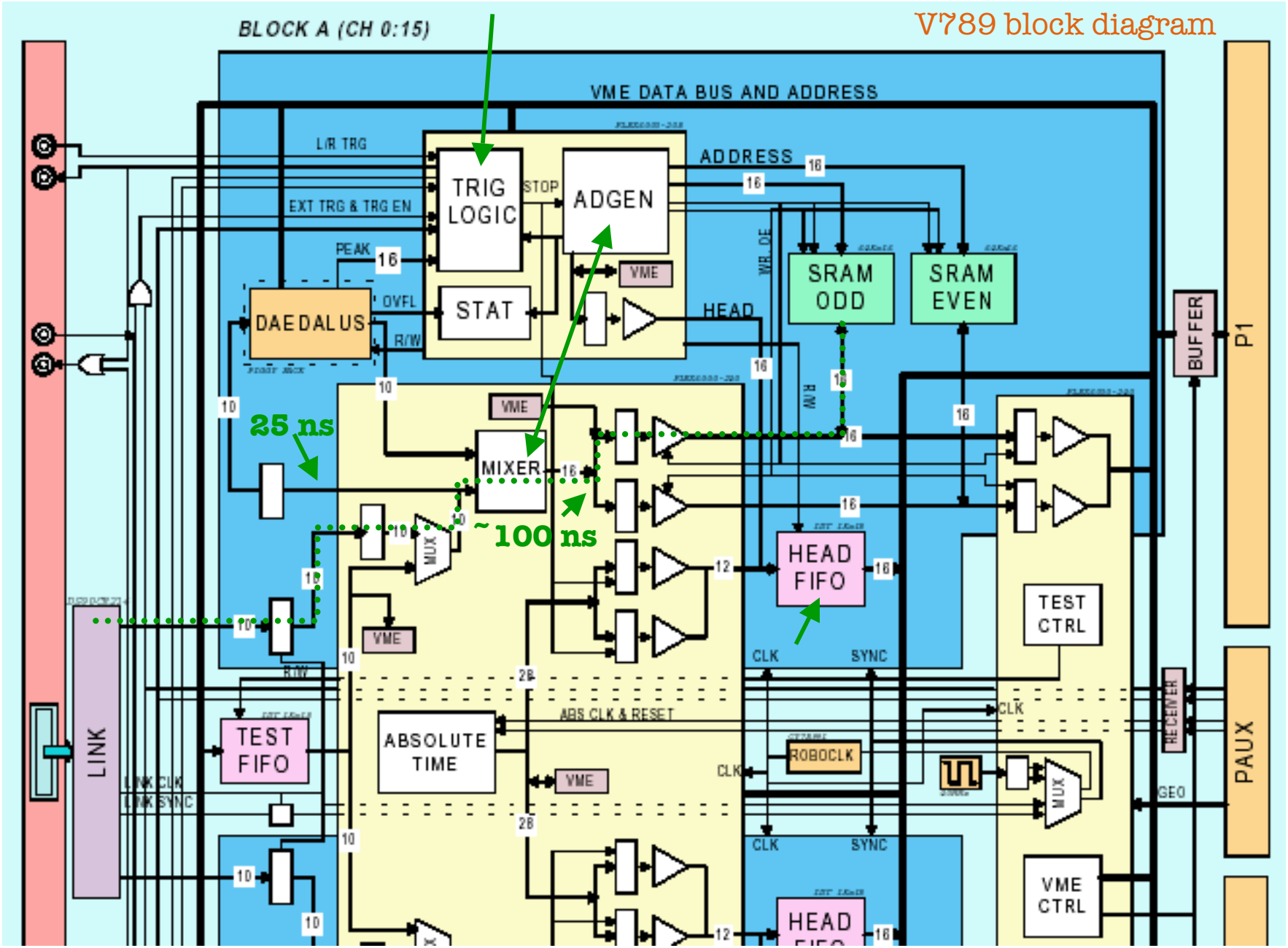
16 new registers needed to carry "previous" values
Writes accesses to RAM must be decoupled in the dataflow
(decimated in average, but abnormal steps might require 5 writes instead of 4)
Total buffer size can become variable
(must be stored to optimize DMA which doesn't decode data)

Difference Coded Compression

Each sample is coded on 4 bits as the difference between itself and the previous sample (throwing daedalus output bits). Should the difference be outside 4-bit boundaries (< 1% of samples), a flag is raised and the full 16 bits value is then used.

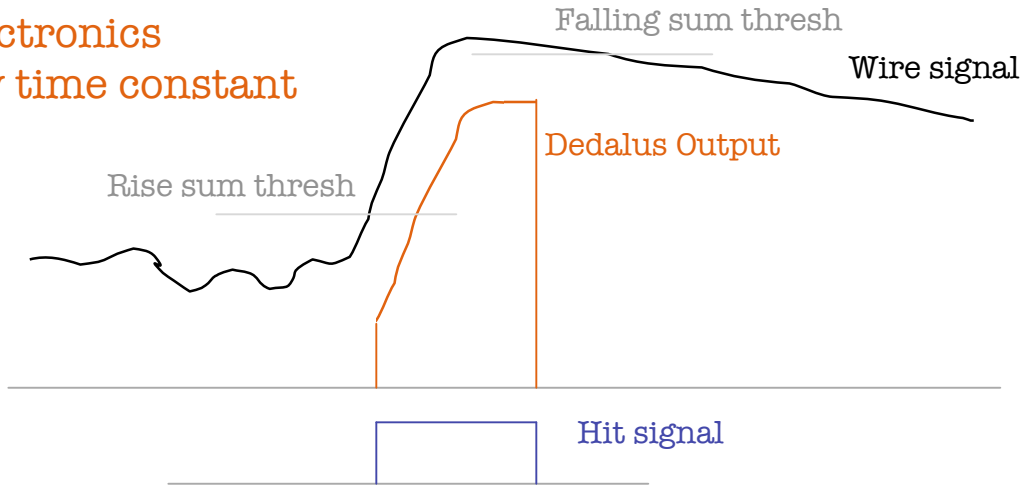


Event Data Format upgrade II



Dedalus Hit Finding upgrade I

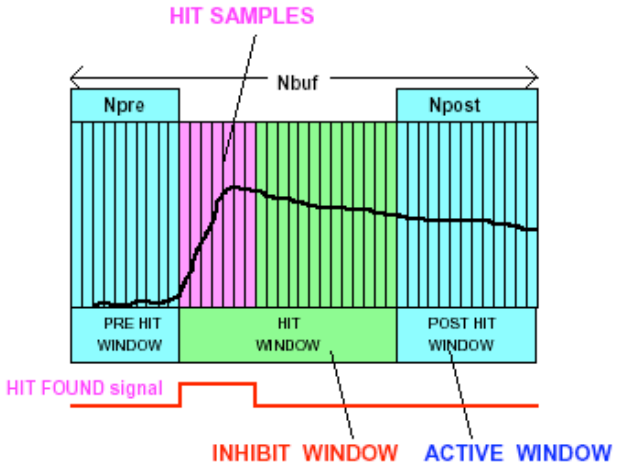
Dedalus hit finding (and its logic)
was designed
when front-end electronics
still had long decay time constant



Its algorithm is aimed to front-edge detection, cutting off baseline to cope with larger fluctuations and signal pileups

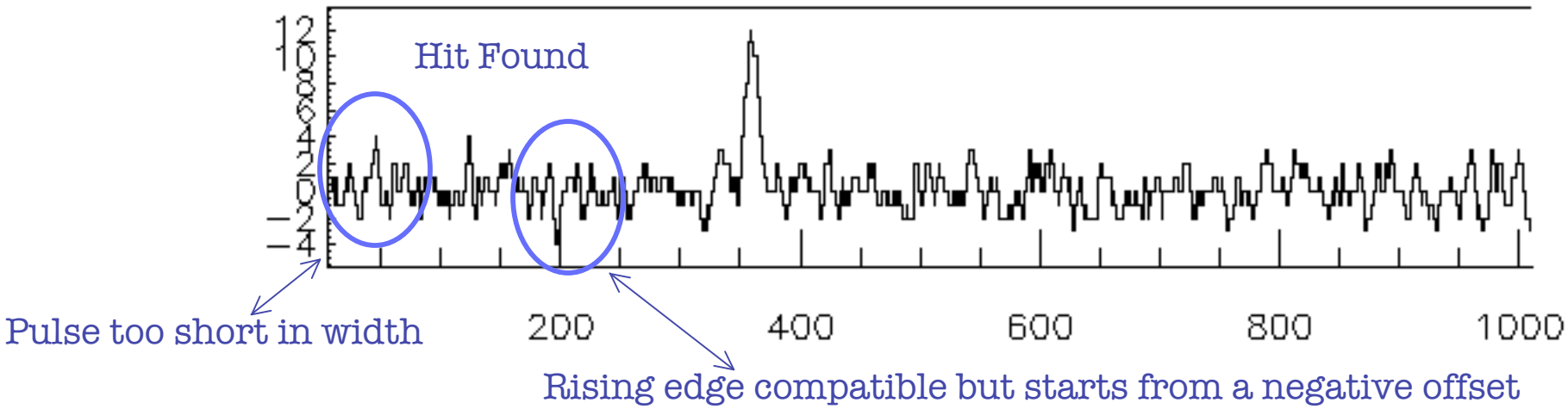
Hit signal starts on front edge detection and lasts for the whole front duration

Trigger logic on V789 considers the hit as soon as Hit signal rises (duration is used only to fulfill post-trigger number of samples)



Dedalus Hit Finding upgrade II

Following this Hit definition, some noise hits get through even if they could be rejected



A different baseline handling would require Dedalus reworking

Dedalus are swappable, but cost is a concern
(an FPGA chip capable to host present Dedalus logic quotes ~200 €)

Discrimination on pulse width could be implemented by the Trigger Logic with a threshold on Hit Signal duration.

Although conceptually just a counter, the threshold integration into the logic could involve a major intervention in the state machine which has to deal with all trigger sources (External Trigger, External Enable, 16 dedalus channels, 2 dedalus neighboor)and their time relations

Good result from software emulation of this threshold on real data

False detections lowered by at least a factor 2 (from 20% to 10%)

A possible upgrade for the V789 firmware

V789 Firmware revision in two steps:

"Reverse Engineering" of the present software to recover
a well defined set of specs & requirements

Porting of the board model into some supported FPGA development framework, with the inclusion of the new illustrated features

A meeting with CAEN foreseen by the end of February to collect all available documentation

Two graduation thesis on this subject are starting in Padova, further help will come from Napoli team